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RFicient®
Ultra-low Power Wake-Up Receiver FH101RF

DATASHEET

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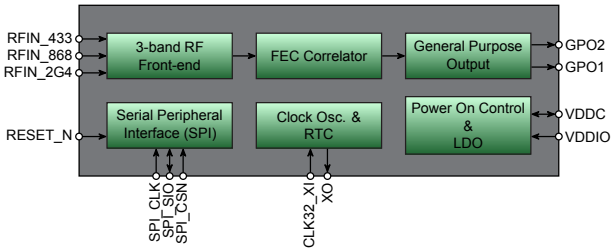
RFicient® Ultra-low Power Wake-Up Receiver FH101RF

Features

- Continuous monitoring of the wireless channel
- Tri-band wake-up and data reception
- 433 MHz, 868 MHz or 915 MHz and 2.4 GHz SRD frequency bands
- Selective wake-up with 16 bit ID via built-in address decoder
- Recognition of two separate wake-up patterns
- Operates with micro-controller in deep sleep mode
- Very low operating current consumption < 3.5 µA
- Response time only 32 ms
- Receiver sensitivity typically −75 dBm
- Separate RF single-ended inputs
- Adjustable receiver data rate
- SPI slave interface to host
- Fault-tolerant data decoding
- Tolerates co-channel interferers with bit-error-rates up to 16 %.
- Operating temperature range:
  T_A = −20 °C to 85 °C
- Very small package and footprint

Applications

- Smart home and building automation
- Remote keyless operations
- Industrial condition monitoring
- Remote wireless control
- Wireless sensor networks
- Body area networks
- Ambient assisted living
- Fitness monitoring
- Asset tracking / Indoor localization
- Telematics
- Vehicle monitoring



PART NAME	PACKAGE	BODY SIZE (NOM)
FH101RF	QFN-16	3 mm × 3 mm

Description

The FH101RF RFicient® Ultra-low Power Wake-Up Receiver is a tri-band receiver for simultaneous reception of OOK modulated signals in the SRD frequency bands 433 MHz, 868 MHz or 915 MHz and 2.4 GHz. It achieves a receiver sensitivity of typically −75 dBm.

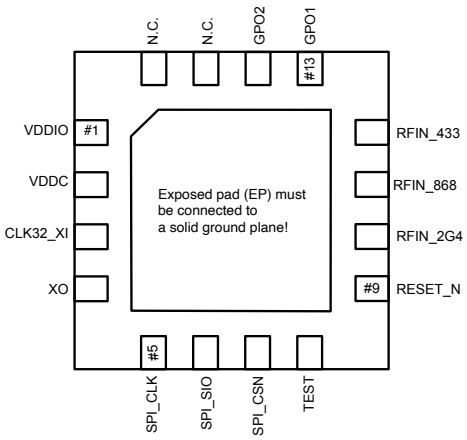
RFicient® receiver technology enables continuous monitoring of a radio channel at microwatt power consumption and responds in milliseconds. This allows mobile applications to operate with 24/7 connectivity and extended lifetime up to 10 years on very small batteries.

The integrated ULP receiver RFicient® operates without the use of a micro controller and recognizes two separate wake-up patterns and a 16 bit ID. After receiving a specific wake-up pattern, a digital control signal is generated to activate any application hardware like a MCU. Hence, individual RF modules can be addressed directly without the need of a wireless sensor network. Moreover, addressing groups is also available.

Data packets can be received by the RFicient® receiver and stored in three built-in FIFO buffers.

All of these data events can trigger an IRQ signal for external circuitry in order to indicate available data. Thus, peripheral components can be run in deep-sleep operating modes and achieve ultra-low values of the total power consumption.

The RFicient® communication uses binary correlators to detect predefined 31-bit preambles. Applying appropriate sequences with excellent auto correlation and cross correlation attributes, the preamble detection can tolerate strong co-channel interferers with biterror-rates up to 16 %.



- QFN-16L Package – Operating Range [−20 °C to 85 °C]
- PB Free, halogen free, RoHS/WEEE compliant product

Contents

1 Pin Configuration and Functions

For additional configuration information see section 8 on device markings and mechanical, packaging, and orderable information.

Pin No.	Name	Type[1]	Description
1	VDDIO	IO Supply (Battery Voltage)	Power Supply 1.8 V to 3.3 V. SPI and GPO will have VDDIO voltage as HI level.
2	VDDC	Core Supply Voltage LDO Output	Core level supply voltages at 1.5 V, generated from LDO or externally supplied
3	CLK32_XI	Clock Input	Crystal connector pin for operation with internal low power clock or system clock input, typically 32,768 Hz for external clock operation.
4	XO	Output	Crystal connector pin for operation with internal low power clock.
5	SPI_CLK	Digital Input	SPI Clock Signal
6	SPI_SIO	Digital In/Out	SPI Slave Input and Output. Note: This is a bidirectional signal.
7	SPI_CSN	Digital Input	SPI Chip Select, Low active
8	TEST	Digital Input	Test Enable, production scan test only. TEST input must be connected to GND for application!
9	RESET_N	Digital Input	Reset to chip default settings, pull down for $t_{reset} = 4T_{CLK\_32}$
10	RFIN_2G4	RF-Input	LNA input, 2.4 GHz band
11	RFIN_868	RF-Input	LNA input, 868 MHz band
12	RFIN_433	RF-Input	LNA input, 433 MHz band
13	GPO1	Digital Output	General Purpose Output 1 (see section 5.5)
14	GPO2	Digital Output	General Purpose Output 2 (see section 5.5)
15	–	–	Not connected, leave open!
16	–	–	Not connected, leave open!
EP	GND	Supply	Connect exposed pad to Ground.

[1] All digital inputs & outputs active high unless otherwise noted.

Table 1: Pin Configuration and Functions.

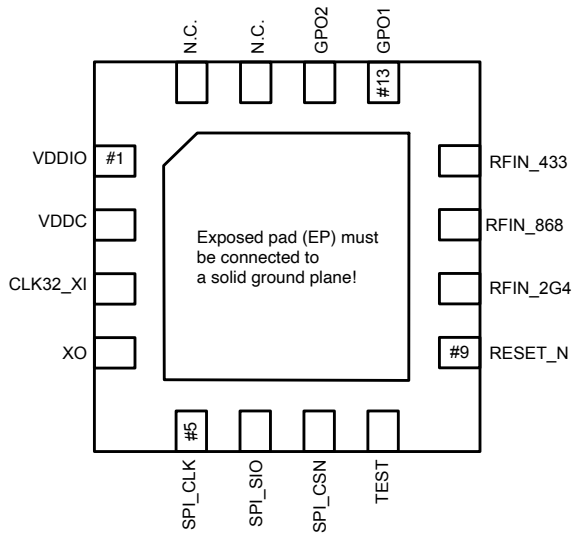


Figure 1: Pin drawing.

2 Electrical Specifications

2.1 Operating Conditions

Tables 2 to 4 list the recommended operating conditions with recommended input levels for typical board-level interface logic levels, i.e. 3.3 V, 2.5 V and 1.8 V. Continuous operation at the VDDIO voltage-level from 3-V lithium-based batteries down to the batteries depletion level at approximately 2.5 V is possible.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage VDDIO	2.97	3.3	3.63	V
Supply Voltage Core VDDC	1.35	1.5	1.65	V
Voltage on digital input/output pins	−0.3		V_{VDDIO} + 0.3	V
Digital HI input level	2		V_{VDDIO} + 0.3	V
Digital LO input level	−0.3		0.8	V
Operating ambient temperature	−20	20	85	°C

Table 2: Recommended operating conditions for 3.3-V-logic.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage VDDIO	2.25	2.5	2.75	V
Supply Voltage Core VDDC	1.35	1.5	1.65	V
Voltage on digital input/output pins	−0.3		V_{VDDIO} + 0.3	V
Digital HI input level	1.7		V_{VDDIO} + 0.3	V
Digital LO input level	−0.3		0.7	V
Operating ambient temperature	−20	20	85	°C

Table 3: Recommended operating conditions for 2.5-V-logic.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage VDDIO	1.62	1.8	1.98	V
Supply Voltage Core VDDC	1.35	1.5	1.65	V
Voltage on digital input/output pins	−0.3		V_{VDDIO} + 0.3	V
Digital HI input level	1.29		V_{VDDIO} + 0.3	V
Digital LO input level	−0.3		0.57	V
Operating ambient temperature	−20	20	85	°C

Table 4: Recommended operating conditions for 1.8-V-logic.

2.2 Absolute Maximum Ratings

Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min.	Max.	Unit
Supply Voltage IO VDDIO	−0.5	3.63	V
Supply Voltage Core VDDC	−0.5	1.65	V
Voltage on digital input/output pins	−0.5	V_{VDDIO} + 0.5	V
Voltage on clock input	−0.5	1.92	V
Voltage on RF-input pins	−0.5	V_{VDDC} + 0.5	V
Input RF level		+10	dBm
Storage temperature	−40	125	°C
Reflow solder temperature		245	°C

Table 5: Absolute maximum ratings.

2.3 Current Consumption

Current consumption of the device depends on various settings. Those settings are sampling rates (sec. 5.6), active frequency bands (sec. 7.1) and the chosen supply and 32,768 Hz clock setups.

2.3.1 External 1.5 V supply and external clock

VDDC voltage and 32,768 Hz clock are supplied externally by the user. This is also called dual-supply mode. Table 6 shows the typical and maximum current consumptions measured at pin VDDC for selected sampling rates and active frequency bands.

reg. value NFA<band>_SLOW	reg. value BAND_BRANCH_CTRL<6:4>	active bands	sample rate per band	T_{LDR}	I_{VDDC} Typ	I_{VDDC} Max
			[bps]	[ms]	[µA]	[µA]
5	0b010	868	1024	31.2500000	3.0	3.8
5	0b100	2G4	1024	31.2500000	2.8	3.5
5	0b001	433	1024	31.2500000	3.1	4.0
5	0b110	2G4/868	1024	31.2500000	4.8	6.7
5	0b011	868/433	1024	31.2500000	5.1	7.3
5	0b101	2G4/433	1024	31.2500000	5.0	6.9
5	0b111	2G4/868/433	1024	31.2500000	7.0	10.2
0	0b100	2G4	32,768	0.9765625	59.9	94.5
0	0b010	868	32,768	0.9765625	64.4	104.3
0	0b001	433	32,768	0.9765625	68.7	110.7
1	0b100	2G4	16,384	1.9531250	30.6	47.5
1	0b010	868	16,384	1.9531250	32.8	52.4
1	0b001	433	16,384	1.9531250	34.9	55.6
2	0b100	2G4	8192	3.9062500	15.8	24.1
2	0b010	868	8192	3.9062500	16.9	26.5
2	0b001	433	8192	3.9062500	18.0	28.1
3	0b100	2G4	4096	7.8125000	8.4	12.3
3	0b010	868	4096	7.8125000	9.0	13.5
3	0b001	433	4096	7.8125000	9.5	14.3
4	0b100	2G4	2048	15.6250000	4.7	6.4
4	0b010	868	2048	15.6250000	5.0	7.1
4	0b001	433	2048	15.6250000	5.3	7.5
6	0b100	2G4	512	62.5000000	1.9	2.9
6	0b010	868	512	62.5000000	2.0	3.0
6	0b001	433	512	62.5000000	2.1	3.1
7	0b100	2G4	256	125.0000000	1.5	2.3
7	0b010	868	256	125.0000000	1.5	2.4
7	0b001	433	256	125.0000000	1.5	2.4

Table 6: Current consumptions in dual-supply mode with external clock at room temperature.

⚠ In this mode the device consumes an additional current of ≈ 0.4 µA from pin VDDIO.

2.3.2 Single supply at VDDIO & internal clock

Internal LDO for VDDC-generation and clock generator are enabled according to sections 5.2 and 5.1, with external crystal and VDDC capacitor. Table 7 shows the current consumptions at pin VDDIO. No additional current is consumed at pin VDDC. The receiver operates fully sustained from VDDIO.

reg. value NFA<band>_SLOW	reg. value BAND_BRANCH_CTRL<6:4>	active bands	sample rate per band	T_{LDR}	I_{VDDIO} Typ	I_{VDDIO} Max
			[bps]	[ms]	[µA]	[µA]
5	0b010	868	1024	31.2500000	4.2	5.8
5	0b100	2G4	1024	31.2500000	4.1	5.5
5	0b001	433	1024	31.2500000	4.4	6.0
5	0b110	2G4/868	1024	31.2500000	6.2	8.9
5	0b011	868/433	1024	31.2500000	6.5	9.5
5	0b101	2G4/433	1024	31.2500000	6.3	9.1
5	0b111	2G4/868/433	1024	31.2500000	8.4	12.6
0	0b100	2G4	32,768	0.9765625	64.5	102.7
0	0b010	868	32,768	0.9765625	69.1	112.5
0	0b001	433	32,768	0.9765625	73.4	118.9
1	0b100	2G4	16,384	1.9531250	33.4	52.5
1	0b010	868	16,384	1.9531250	35.7	57.4
1	0b001	433	16,384	1.9531250	37.8	60.6
2	0b100	2G4	8192	3.9062500	17.8	27.5
2	0b010	868	8192	3.9062500	18.9	29.9
2	0b001	433	8192	3.9062500	20.0	31.5
3	0b100	2G4	4096	7.8125000	10.0	14.9
3	0b010	868	4096	7.8125000	10.5	16.1
3	0b001	433	4096	7.8125000	11.1	16.9
4	0b100	2G4	2048	15.6250000	6.0	8.6
4	0b010	868	2048	15.6250000	6.3	9.3
4	0b001	433	2048	15.6250000	6.6	9.7
6	0b100	2G4	512	62.5000000	3.1	3.9
6	0b010	868	512	62.5000000	3.2	4.1
6	0b001	433	512	62.5000000	3.2	4.2
7	0b100	2G4	256	125.0000000	2.6	3.2
7	0b010	868	256	125.0000000	2.6	3.2
7	0b001	433	256	125.0000000	2.6	3.3

Table 7: Current consumptions in single-supply mode with internal clock generation at room temperature.

2.3.3 Current consumption vs. temperature.

Figure 2 shows the measured typical current at VDDIO in single supply mode dependent on ambient temperature, with and without internal clock generator.

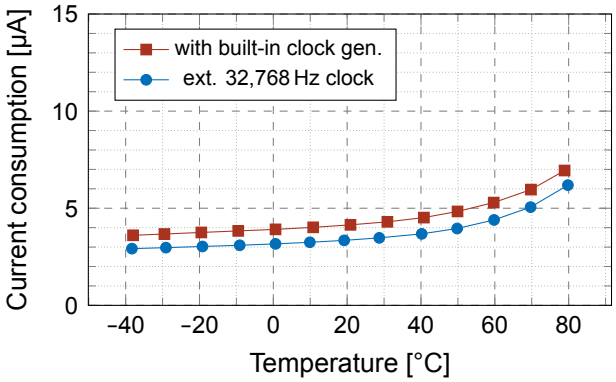


Figure 2: Typical current consumption over temperature.
Settings after Reset and power-up procedure (cf. sec. 5.7): Default (LDR 1024 bps), SPG_CAL executed (cf. sec.7.3.3), BAND_BRANCH_CTRL = 39 (i.e. 868 MHz).

2.4 Sensitivity

Typical sensitivity values dependent on the receiver's operating frequency are given in table 8.

SRD band [MHz]	Typ. Sensitivity [dBm]
433	−75
868 / 915	−75
2400	−72

Table 8: Measured typical sensitivity at different ports. Condition: Calibration at room temperature, and COMP_THRESH_W = 10

In order to minimize receiver sensitivity variation over the specified temperature range (table 2), it is required to repeatedly execute the calibration routines described in section 7.3. Depending on the application and expected temperature changes calibrations should be executed every few minutes or up to once per hour; or with the availability of environmental temperature data every 10 °C. Figure 3 shows the receivers typical sensitivity over temperature, if calibrations are executed at every shift of 10 °C in temperature.

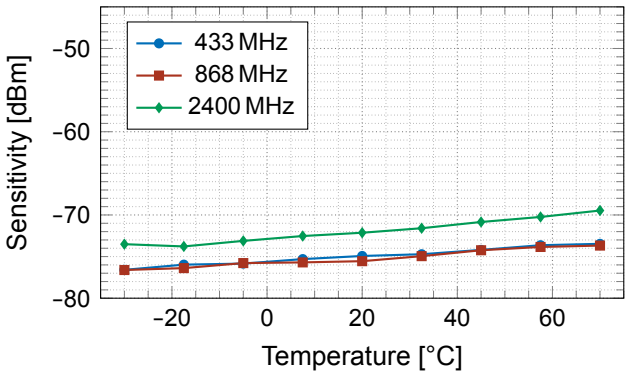


Figure 3: Typical sensitivity over temperature.
All calibrations executed every 12.5 °C (cf. sec.7.3).

2.5 Input matching

Table 9 shows the receivers complex input impedances. Antennas or SAW filters have to be matched to the given impedances, depending on the application circuit and board-parameters.

		Input Impedance Z_{RFIN} [Ω]	
Input Pin	**Frequency** [MHz]	**Real Component**	**Imaginary Component**
RFIN_433	433	80.6	-189
RFIN_868	868	50.3	-121.9
RFIN_2G4	2400	18.7	-52.3

Table 9: Measured typical input impedance at package level.

2.6 ESD Ratings

Parameter	**Charge Model**	**Min**	**Max**	**Unit**	**Pins**
Input current (Latch-up immunity)		-100	100	mA	
V_{ESD} Electrostatic discharge	HBM[1]		±1500	V	All Pins except RF Pins
	HBM[1]		±500	V	RF Pins 10, 11, 12
	CDM[2]		±1000	V	All Pins except RF Pins
	CDM[2]		±350	V	RF Pins 10, 11, 12

[1] Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 - JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
[2] Charged device model (CDM), per JEDEC specification JESD22-C101 - JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

3 General description

3.1 The RFicient® ULP receiver technology

The RFicient® Wake-Up receiver is a tri-band receiver for simultaneous reception of OOK (on-off keying) modulated signals in the SRD frequency bands 433 MHz, 868 MHz or 915 MHz and 2.4 GHz. It achieves a receiver sensitivity of typically −75 dBm.

RF band selection is done tuning the RX frequency and in addition with an external SAW filter. The receiver offers separated RF single-ended inputs for each frequency band at a high grade of flexibility. Applications can run with single, double or multi-band antennas depending on the individual requirements.

When operating in the standard single-band configuration at a data rate of 1 kbit/s, the current consumption is approximately 3 µA at an externally supplied core voltage of 1.5 V and an additional 0.4 µA at the a supply of 1.8 V to 3.3 V for CMOS-level bus-communication. The response time in this case is only 32 ms.

The data rate for each RF band can be adjusted individually. The user can choose single-band, dual-band or tri-band among operating modes during runtime. All configurations are set via the SPI interface. The receiver works as RF monitoring circuit that delivers IRQ events for connected micro-controllers (MCU's) due to the incoming RF telegrams. Furthermore, user specific data packets can be received and read out in the FIFO memory for each frequency band simultaneously. An external 32,768 Hz clock source is needed or can be provided from the built-in sub-1-µA crystal oscillator with an external clock crystal.

An internal low drop-out (LDO) voltage regulator can generate the core voltage from a 1.8 V to 3.3 V external battery voltage. Utilizing the internal ULP clock generator circuit with an external quartz crystal and the internal LDO the current consumption increases slightly to only 4.2 µA at 1 kbit/s sampling rate and one sampled RF-band. The lowest current consumption for the receiver is approximately 1.5 µA for single-band operation and lowest sampling rate. More available sampling rates and band-selection combinations are shown in section 2.3.

The integrated ULP receiver RFicient® operates without the use of an external micro-controller and recognizes two separate wake-up patterns. After receiving a specific wake-up pattern, a digital control signal is generated to activate any application hardware like a MCU.

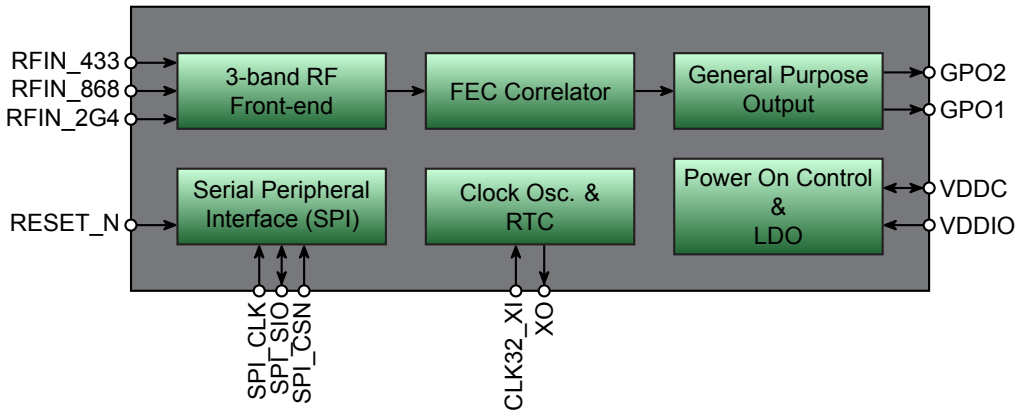


Figure 4: Block diagram of the receiver.

3.2 Fault-tolerant Preamble Detection

Applying fault-tolerant data decoding, the RFicient® receiver provides a robust unidirectional data communication. This is suitable for remote control or remote sensor applications. The On-Off-Keying

(OOK) modulation was chosen for power consumption reasons. Moreover, OOK schemes require fault-tolerant data decoding without bidirectional communication. Thus, the RFicient® communication uses binary correlators to detect predefined 31-bit preambles. Applying appropriate sequences with excellent autocorrelation and cross-correlation attributes, the preamble detection can tolerate strong co-channel interferers with bit-error-rates up to 16 %. A pair of 31-bit correlators are continuously fed with incoming OOK symbols provided from the ultra-low power analog front-end for each frequency band. Within the RFicient® receiver, six binary correlators are implemented to provide simultaneous and independent tri-band data reception. The specified values for the receiver current consumption comprise both the analog front-end and the digital processing of the correlators, address and data decoders.

3.3 Selective Wake-up: Built-in Address Decoder

Apart from the pure wake-up mode of operation, a selective activation using a 16-bit wide address range and reception of coded data streams is possible. The RFicient® receivers scans up to three selected RF bands for incoming wake-up telegrams. These can be interpreted from the receiver as selective wake-up address. Hence, individual RF modules can be addressed directly without the need of a wireless sensor network. Addressing groups is also available. From the network perspective, a particular broadcast address, that is assigned to a certain radio network, can be used to address all items of one common network.

Data packets can be received by the RFicient® receiver and stored into three built-in FIFO buffers. This can be combined with selective wake-up addressing. All of these data events can trigger an IRQ signal for external circuitry in order to indicate available data. Thus, peripheral components can be run in deep-sleep operating modes and achieve ultra-low values of the total power consumption. A more detailed description of the underlying protocol is given in section 5.6.

3.4 Fast Data Decoder

The RFicient® receiver can be run at a very low current consumption if the data rate is set to 1.024 kbit/s or lower. Recognizing a certain wake-up preamble in this so-called low-data-rate (LDR) mode, the receiver by default switches the data rate to a predefined higher value for high data rate (HDR) operation, e.g. 8.192 kbit/s. As soon as the data packet is fully received at the higher data rate, the receiver reduces the data rate to the original lower value (LDR mode). Hence, the average current consumption remains constantly low for rare data events. This allows the user to combine ultra-low power radio reception of short messages with low latencies. The collected decoded bits are stored into a FIFO buffer with possible lengths between 16 bit to 40 bit. If the FIFO buffer is filled, the receiver can generates an IRQ signal automatically. Thus, the user's MCU can pick up the collected data packet at once.

Frequent wake-up events with data transmission in FDD-mode (e.g. every second) can increase the average current consumption of the receiver. A more detailed description is given in section 5.6.2.

3.5 Built-in Calibration Circuits

The receive frequencies and internal comparator thresholds mostly suffer from power supply and temperature variations. Therefore, several calibrations are integrated within the RFicient® receiver. Avoiding the need for further external reference signals, the built-in calibrations use the crystal frequency from the 32,768 Hz clock source. The user can initiate frequency and threshold calibrations at any desired point of time. Doing this during the receiver runtime, the reception is interrupted for less than ten milliseconds. Moreover, a third calibration is implemented and optimizes internal timing sequences. A detailed description of calibration control mechanisms is given in section 7.3.

3.6 Fast Register Access via SPI

Reading and writing the RFicient® receiver configuration settings, data buffers, interrupt settings, event buffers and calibration data is carried out via SPI (serial peripheral interface). Enabling very short operating times for peripheral MCUs, the SPI clock frequency is designed to be as high as 10 MHz. Thus, each register transfer may need less than two microseconds. Wireless tags which require very small reaction times benefit from this.

3.7 IRQ generation: Data Events and RTC Timer Events

The user can choose between several possible events for automatic IRQ signal generation: Wake-up sequences A or B, FIFO buffer filled, FIFO buffer overflow, ID match. The SPI_SO/IRQ signal is set high if a specified event occurs. A 4-bit SPI register indicates the event type. Several built-in user-defined timers help to implement complex and accurate data protocols.

3.8 Evaluation Kits

Ready-to-use evaluation kits including software suites are available upon request via distributor EBV Elektronik at: https://www.avnet.com/wps/portal/ebv/solutions/ebvchips/rficient/.

4 Typical Application Circuit

Figure 5 depicts an exemplary application circuit for use case of the RFicient® receiver with all available frequency bands, using the internal LDO and clock generator with a quartz crystal X1 and an external SAW-filters for the 868-MHz and 433-MHz bands[1]. An external micro-controller and battery (e.g. coin cell CR2032) are not shown in the schematic. Recommend component values and manufacturer numbers for this circuit are given in table 10.

The passive devices for input matching of the RF ports are chosen for an exemplary PCB design, which can be requested via contact information provided at http://rficient.com. If the customer requires a custom PCB design, calculation of the RF input matching network should be performed with input impedances given in table 9. These are measured at the package level.

Unneeded RF ports can be left open. Ensure the corresponding bands are deactivated with register BAND_BRANCH_SELECT (see section 7.1). For mounting options of the external crystal for the internal crystal oscillator refer to section 5.1.

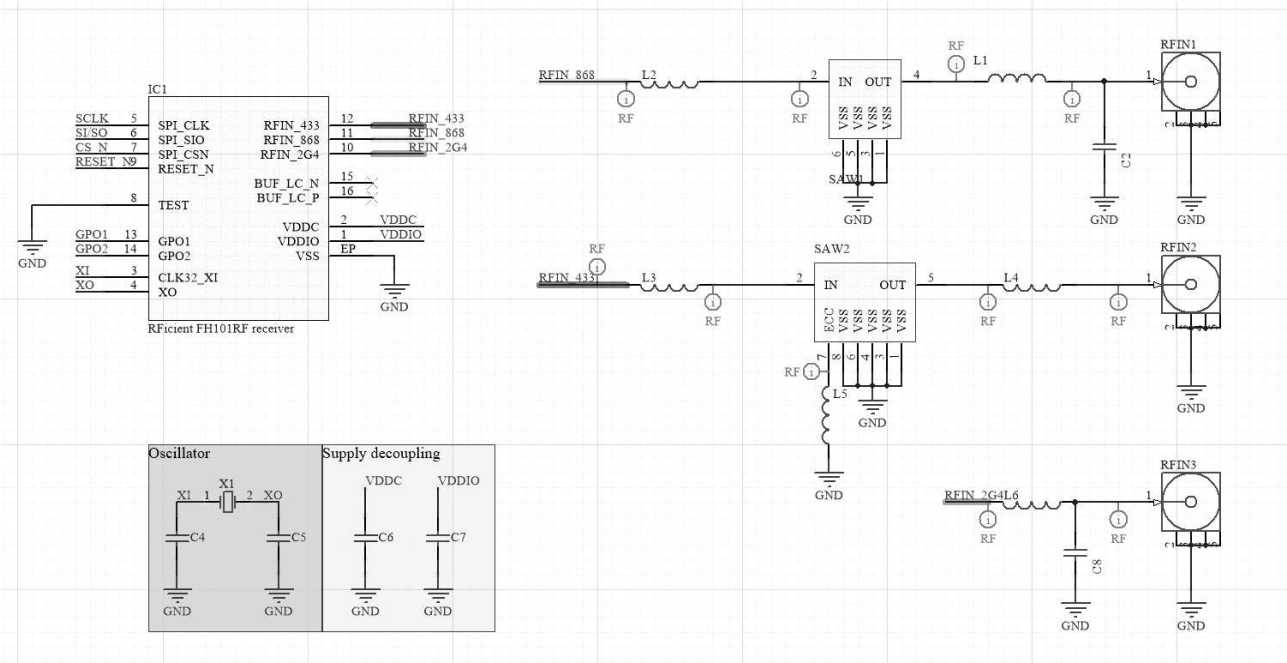


Figure 5: Typical application circuit for UHF tri-band operation.

[1]Narrow-band SAW solutions for the 2.4-GHz-band are currently not commercially available, but will be added as soon as available.

Identifier	Value	Description	Manufacturer Number
C2	2 pF	Multilayer Ceramic Capacitors MLCCSMD/SMT 50 V2 pF Ultra High Q NPO	500R07S2R0BV4T
C4, C5	10 pF	Multilayer ceramic capacitors MLCC - SMD/SMT 50 V 10 pF C0G 0201 5 %	02015A100JAT2A
C6	4.7 µF	Multilayer ceramic capacitors MLCC - SMD/SMT 4.7 µF ±20 % 10 V X7R 0805	LMK212B7475MGHT
C7	100 nF	Multilayer ceramic capacitors MLCC - SMD/SMT 100 nF 5 % 25 V	CC0402JRX7R8BB104
C8	1.8 pF	Multilayer ceramic capacitors MLCC - SMD/SMT 50 V 1.8 pF Ultra High Q NPO	500R07S1R8BV4T
IC1	–	RFicient FH101RF	–
L1	22 nH	Coilcraft Fixed inductors 0603 22 nH 5 % 900 mA 0.095 Ω	0603DC-22NXJRW
L2	30 nH	Coilcraft Fixed inductors 0603 30 nH 5 % 900 mA 0.103 Ω	0603DC-30NXJRW
L3	110 nH	Coilcraft Fixed inductors 0603 110 nH 5 % 270 mA 0.725 Ω	0603DC-R11XJRW
L4, L5	56 nH	Coilcraft Fixed inductors 0603 56 nH 5 % 470 mA 0.26 Ω	0603DC-56NXJRW
L6	2.8 nH	Fixed inductors 0402 2.8 nH Hi-Q SMD RF IND	LQW15AN2N8C00D
SAW1	868.3 MHz	SAW filter 868.3 MHz	B39871B3744H110
SAW2	433.9 MHz	SAW filter 433.9 MHz	B39431B3790Z810
X1	32,768 Hz	Crystals 32.768 kHz 9 pF −40 °C to 85 °C	ECS-.327-9-12R-C-TR

Table 10: Recommended passive components referring figure 5.

5 Operational Description

5.1 Crystal Oscillator

Summary

- Built-in 32,768 Hz real time clock crystal oscillator
- Characterized with crystal loading capacitors ranging from 4 pF to 20 pF
- Low power design (< 1.2 µW typical) operates on core VDD only
- I_{avg} < 0.8 µA (typical model, 25 °C)
- P_{leak} ≈ 75 nW (typical model, 25 °C)
- Oscillator enable/disable via SPI register
- Oscillator tuning via SPI register

Detailed Description

The product is equipped with an ultra low power oscillator suitable for 32,768 Hz clock quartz crystals. Pins CLK32_XI and XO have to be connected to the quartz crystal for oscillator operation. Table 11 lists recommended quartz crystals. Make sure to provide two additional capacitors C4 and C5 to satisfy C_{Load} specifications.

No.	Part Number	Mount Type	Drive Level	C_{Load} [pF]	C_{Shunt} [pF]	Form Factor [mm^3]
1	ECX-.327-CDX-1293	SMD	100 nW, max. 1 µW	12.5	1.1	3.2 x 1.5 x 0.9
2	ECS-.327-9-12R-C-TR	SMD	max. 1 µW	12.5	1.3	2 x 1.2 x 0.6
3	LFXTAL009709 Bulk	SMD	max. 1 µW	7	1.1	3.2 x 1.5 x 0.5
4	LFXTAL002995 Bulk	Cylinder	max. 1 µW	12.5	2.5	3.0 x 8.0

Table 11: Recommended quartz crystals for built-in clock oscillator.

Enabling the crystal oscillator is controlled via register setting. When disabled, an external system clock can be fed to the CLK32_XI pin. XO is left open in this case, i.e. the bypass mode.

⚠ In case of an external clock the high signal level signal at pin CLK32_XI must not exceed the core supply (VDDC) voltage level.

In a later version, the crystal oscillator will be digitally tunable via register setting to correct the clock-drift of the real time clock counter (RTC). For operating instructions of the RTC see section 7, description of registers.

Recommended values for C4 and C5 are C4 = C5 ≈ 2(C_{Load} − C_{Shunt} − 1 pF). C_{Shunt} and C_{Load} depend on the chosen crystal device, according to table 11

Parameter	Description	Min.	Typ.	Max.	Unit
VDDC	Core supply voltage	1.35	1.5	1.65	V
VDDIO	I/O supply voltage Options	2.97	3.3	3.63	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
T_j	Junction temperature	−40	25	85	°C
V_{CLK32_XI}	Voltage at CLK32_XI		1.5		V

Table 12: Recommended operating conditions for oscillator.

5.2 Low-Drop-Out Regulator

Summary

- Built-in low-drop-out voltage regulator to generate VDDC at 1.5 V from battery voltage VDDIO
- Quiescent current I_Q < 400 nA (typ. at VDDIO pin)

Detailed Description

A built-in LDO provides the option to supply the receiver from a single voltage supply between 1.8 V to 3.3 V, e.g. from a battery. A regulated 1.5 V core voltage is generated by the LDO. An internal bandgap circuit operates as voltage reference for the regulator. Due to fast sampling operation the quiescent current I_Q of the LDO is less than 400 nA on average. The LDO adjusts the core voltage periodically in pulse operation. The residual voltage deviation is kept below 10 mV for 1.5 V typical core voltage. External 4.7 µF and 100 nF capacitors are needed for stabilization at the VDDC and VDDIO supply pins, respectively. The equivalent series resistance of the capacitor must be lower than 100 mΩ for frequencies above 1 kHz. Lithium type button cells are recommended as voltage supply. The internal resistance of the applied battery must not exceed 10 Ω, as current peaks of ≈ 3 mA to 5 mA are drawn from VDDIO every time sample to supply the receiver, depending on adjusted data rates in the three RF bands.

The LDO also manages power-up procedures of the receiver and of the built-in crystal oscillator. Stable operation after settling processes is ensured.

The built-in start-up circuitry — i.e. battery voltage surveillance at VDDIO — is always active and consumes less than 350 nA continuously from the VDDIO pin.

Chipdefault is to enable the LDO at start-up. It can be disabled by setting bit 5 in register 0x74 LDO_XTAL_CTRL to 1 (i.e. LDO_ENA_N = 1).

⚠ The LDO *must not* be loaded with circuitry other than the RFicient® wake-up receiver and the specified external decoupling capacitors C6 and C7 at pin VDDC (Fig. 5), as its maximum supply current is optimized only for normal receiver operation and start-up.
During startup the maximum current drawn from the battery supply at VDDIO is limited to 5 mA, in order to not overload the battery. The node VDDC with its connected capacitance is charged with 1 mA to 3 mA. A more detailed description of the start-up procedure is given in section 5.7 of this document.

5.3 Extended Interrupt Generator

Summary

- Eight independent interrupt events selectable by user
- Built-in ID address decoders for wake-up events
- individual wake-up using 16-bit node ID,
- group wake-up or general (“broadcast”) wake-up.
- status of RX data buffer (“FIFO”) can trigger interrupt events
- four built-in RTC timers can trigger alarm interrupts for user-defined timings within protocols
- programmable cyclic timer for periodical interrupts
- Built-in 40-bit clock counter

Description

The product uses 8 predefined interrupt types. If signal pin GPO1 is configured to output IRQ_EVENT (table 13) each of these events will cause a rising edge at this pin. The IRQ event type can than be read out from register 0x32 IRQ_STATUS and identified with event type definitions according to table 13. In order to clear the IRQ event, the flag corresponding to the event must be set in IRQ_CLR register. An exemplary flow for IRQ handling is given in section 7.7 of this document.

Event No.	Event Name	Event Description
0	ID match	16-bit ID (Reg. 0x35, 0x36: ID_HI & ID_LO) in FDD mode fits to received Fast Data Packet
1	FIFO overflow	indicates FIFO overflow if FDD data bits extend the specified FIFO length (Reg. 0x56): 16/24/32/40 bit.
2	FIFO buffer filled	indicates that FIFO is filled with FDD data bits according to the specified FIFO length (Reg. 0x56): 16/24/32/40 bit.
3	Correlation pattern match	OOK data matches the selected correlation sequences (irrespectively of FDD or LDR mode being active)
4	ID match & FIFO filled	event type 0 occurred within the last <FIFO_length +2> bit cycles and event type 2 occurred after event type 0 (“telegram received”)
5	ID match & LDR	event type 0 occurred within the current FDD data reception and transition from HDR to LDR sampling mode occurred after event type 0 (“end of telegram”)
6	RTC Timer Alarm	one of the 4 RTC timers (RTCSH0, RTCSH1, RTCLG0, RTCLG1) have reached the user-defined targets and caused alarm. Register RTC_EVENTS indicates which alarm rings.
7	Cyclic Timer Alarm	the cyclic timer has reached the user-defined target and caused alarm

Table 13: Available interrupt event types.

5.4 Real-time Clock and Built-in Timers

Summary

- The built-in clock offers unique time stamps for one full year
- User-defined timing schemes can be triggered by five built-in timers:
  - ☐ Two short timers up 2 seconds
  - ☐ Two short timers up to 1 year and 23 days
  - ☐ One cyclic alarm timer up to 8 min and 30 seconds

Description

The RFicient® receiver offers a 40-bit clock counter as a built-in system clock that counts 1 year and 23 days before overflow. Derived from that, four user-defined RTC timers are provided with a granularity of 30.517,578 µs (i.e. 1 clock cycle).

Name	Function	Event Description
RTCSH0	16-bit short-term timer	Single Timer with a max. duration of 1.999,964,95 s (i.e. 65,535 clock cycles)
RTCSH1	16-bit short-term timer	Single Timer with a max. duration of 1.999,964,95 s
RTCLG0	40-bit long-term timer	Single Timer with a max. duration of 33,554,432 s (i.e. 388 d 8 h 40 min 32 s)
RTCLG1	40-bit long-term timer	Single Timer with a max. duration of 33,554,432 s
CYCL	16-bit cyclic timer	Provides periodic alarms out of the system clock divided by a factor M, with $1 \leq M \leq 255$. Thus, a maximum alarm period of 8 min 29.9922 s (i.e. 16,711,425 clock cycles) can be adjusted.

Table 14: Available RTC timers.

5.5 Multipurpose Signal Outputs

The RFicient® receiver offers numerous internal signals that are multiplexed to the two output pins GPO1 and GPO2. Writing register 0x75 (MUX_D_OUT_SEL), the user can choose according to table 15. Selecting an output combination with any of the signals COMP_OUT_W/M/S, RX_ACTIVE or CLK32, can increase the devices average current consumption by several micro-amperes. They are intended for test-purposes mainly. It is recommended to use the chip default (15), handling IRQ events by waking a microcontroller using the interrupt-signal IRQ_EVENT.

MUX_D_OUT_SEL	GPO1 Output Signal	GPO2 Output Signal	Description
0	FAST_CLK_2G4	FAST_DATA_2G4	RX data stream at 2.4 GHz
1	FAST_CLK_868	FAST_DATA_868	RX data stream at 868 MHz
2	FAST_CLK_433	FAST_DATA_433	RX data stream at 433 MHz
3	WUP_A_2G4	WUP_B_2G4	Wake-up A/B signals at 2.4 GHz
6	ID_MATCH	WUP_A_433	General ID match, WakeUp signal
7	WUP_A_868	WUP_B_868	Wake-up A/B signals at 868 MHz
8	WUP_A_433	RX_ACTIVE	Wake-up A signal, trigger signal
9	WUP_A_868	RX_ACTIVE	Wake-up A signal, trigger signal
10	WUP_A_2G4	RX_ACTIVE	Wake-up A signal, trigger signal
14	CLK32	IRQ_EVENT	System clock, Interrupt signal
15 (chip default)	IRQ_EVENT	Logic HI (”1”)	Interrupt signal, static high signal

Table 15: Output selection table for GPO1/GPO2 signals.

5.6 RFicient® Protocol: Reception of ID and User Data

Many wireless applications can be distinguished between “RF wake-up” and “RF data reception”. In challenging wireless applications spontaneous wake-up events require both a low system latency (e.g. ≤ 32 ms) and a low current consumption (e.g. ≤ 5 µA). The RFicient® wake-up receiver offers ultra-low current consumption at a low latency at the same time. Consequently, long-term battery-driven applications achieve several years of operation with a single battery and keep RF connected continuously.

A common use case is the detection of an RF wake-up event followed by a short radio telegram

containing an ID, remote instructions and configuration parameters. In order to reduce the current consumption, it is recommended to apply a low data rate for the initial RF wake-up event (preamble). The following user data should be processed very quickly, i.e. at a high data rate in order to occupy the radio channel only for a short time. RFicient® may provide both functions:

1. wake-up reception and
2. ID and data reception.

It is useful for wireless networks when wake-up calls offer selectivity among numerous other RF nodes. Thus, RFicient® technology features three kinds of selective wake-up methods: individual wake-up, group wake-up and broadcast wake-up.

The aforementioned features require a predefined scheme that is included in the two-stage RFicient® protocol according to figure 6.

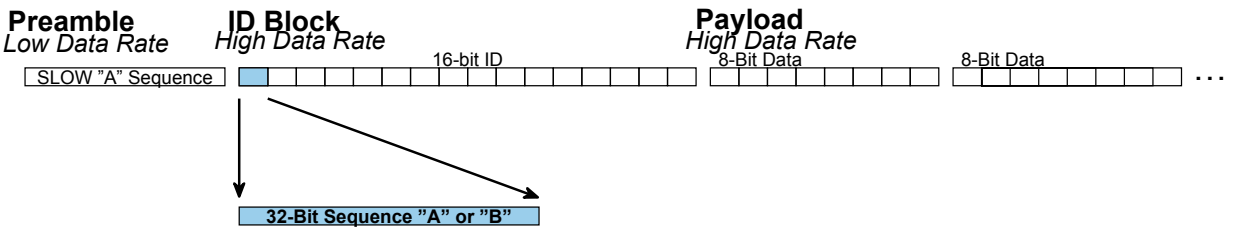


Figure 6: Two-stage RFicient® wireless protocol

The user can enable the fast data decoder (FDD) for each frequency band using register FDD_ENABLE. Consequently, the RFicient® receiver interprets incoming Code A sequences at the low data rate as initiator/preamble for FDD packets sampled at the high data rate. The low and high data rates are set for each frequency band by registers 0x00 to 0x02 NFA<band>_SLOW and registers 0x03 to 0x05 NFA<band>_FAST accordingly.

When in high data rate mode, the receiver interprets incoming Code A sequences as logical “0” and Code B sequences as logical “1”. This ensures a bit error tolerant reception of data packets for a robust unidirectional data communication. Low data rate sequences are ignored in high data rate mode, as well as sequences in data rates other than the selected sampling rate according to register NFA<band>_FAST. Having properly received the 16-bit ID, the receiver compares this with the local ID of the receiver node (see registers 0x35, 0x36). In case of an ID match, an interrupt event “ID match” will be triggered and further incoming “fast mode” data bits are stored in the FIFO data buffer for each frequency band separately. If no further fast data mode bits are received, the receiver will quit fast data mode and switch back to low data rate (LDR). Timeouts for the fallback to the LDR mode are given in table 16 in the next section. The user can choose if this end-of-data event will cause an interrupt.

5.6.1 Timeout

The receiver automatically exits high data rate (HDR) mode if no more bits are properly received in HDR or if no bit is decoded after Code A in HDR mode. Figure 7 illustrates and denotes the timings for a properly received preamble in low data rate and a high data rate data packet of 16 chips (2 bytes), 1 chip comprised of code A or B. The receiver switches into high data rate sampling immediately after the preamble is fully received and switches back to low data rate, if no more bits are sampled within interval T_{P2} min. If no chip (e.g. code A or B) is received within interval T_{P1} min, after the end of the preamble, the receiver also switches back to low data rate sampling.

In both cases, the receiver switches back to LDR sampling and applies the low data rates configured by NFA<band>_SLOW in registers 0x00<2:0>, 0x01<2:0>, 0x02<2:0> again. The respective timeout

periods depending on the data rate in HDR mode are given in table 16. Note: The user can also force the receiver to switch back to LDR mode by setting bit 7 in the registers 0x00, 0x01 or 0x02 respectively.

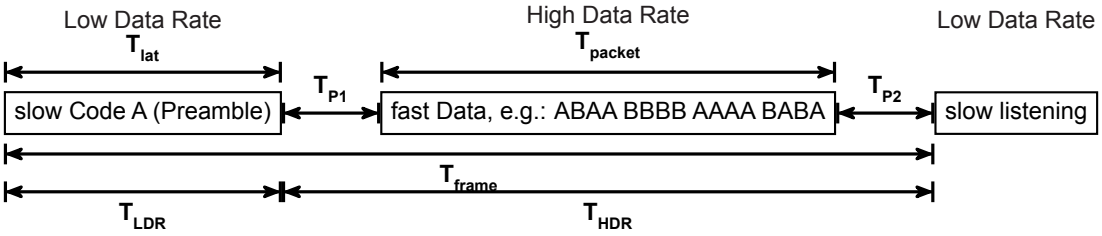


Figure 7: Diagram: Timeout Slots

		No Timeout		Safe Timeout	
NFA<band>_FAST	High Data Rate (HDR) [Hz]	T_{P1} max. [ms]	T_{P2} max. [ms]	T_{P1} min. [ms]	T_{P2} min. [ms]
0	32,768	5.371	1.465	5.432	1.526
1	16,384	10.742	2.930	10.803	2.991
2	8192	21.484	5.859	21.545	5.920
3	4096	42.969	11.719	43.030	11.780
4	2048	85.938	23.438	85.999	23.499
5	1024	171.875	46.875	171.936	46.936
6	512	343.750	93.750	343.811	93.811
7	256	687.500	187.500	687.561	187.561

Table 16: Timeout values for ID- and data transfer.

Example Assuming the low data rate of 1024 bit/s and 32,768 bit/s as high data rate, the preamble duration is 31.25 ms. Each fast user bit is represented by a fast code sequence (chip “A” or “B”) and takes 0.977 ms each. Thus, the 16-bit ID is transmitted within 15.625 ms. An additional payload of 8-bit data packets takes 7.813 ms. An entire frame starting with slow “A”, followed by a transmitter pause P1 of e.g. 1 ms, a 16-bit ID and two 8 bit data packets yield a total frame duration of T_{frame} = 65.026 ms, including the safe timeout T_{P2}, for the receiver to switch back in low data rate and be ready to receiver the next wake-up-message (preamble plus possible data), with T_{P2} = 1.526 ms.

5.6.2 Maximum Packet Rate and Current Consumption

Enabling the FDD reception mode the receiver’s current consumption becomes a function of the frame reception rate r_{frame}, due to the high data rate sampling mode.

It is given with

$$I_{avg}(r_{frame}) = \left[I_{HDR} T_{HDR} + I_{LDR} \left(\frac{1}{r_{frame}} - T_{HDR} \right) \right] r_{frame}, \quad (1)$$

where I_{LDR} and I_{HDR} are the current consumptions of the receiver in low and high data rate mode (cf. tables 6 and 7) and T_{HDR} is the time duration of the receiver in HDR mode as indicated in figure 7. The maximum rate at which wake-up-messages can be received is

$$r_{frame,max} = \frac{1}{T_{frame}}, \quad (2)$$

where T_{frame} marks the time from the beginning of the preamble to the end of HDR mode, as indicated in figure 7. Current consumption peaks at the maximum packet rates according to equation 1 at

$I_{avg}(r_{frame,max})$. Smaller LDR data rates and higher payload correspond to longer frame durations T_{frame} and therefore the number of packets per seconds is limited.

Example Assuming a packet length T_{packet} comprised of 8 bytes[2] and a high data rate (HDR) of 8192 bps, figure 8 shows the average current consumption vs. various average packet rates over a day, for low data rates of 256 bps and 1024 bps and all three receiver bands in single band operation, with internal LDO and clock generator enabled. At the maximum current value, there is no pause between each frame.

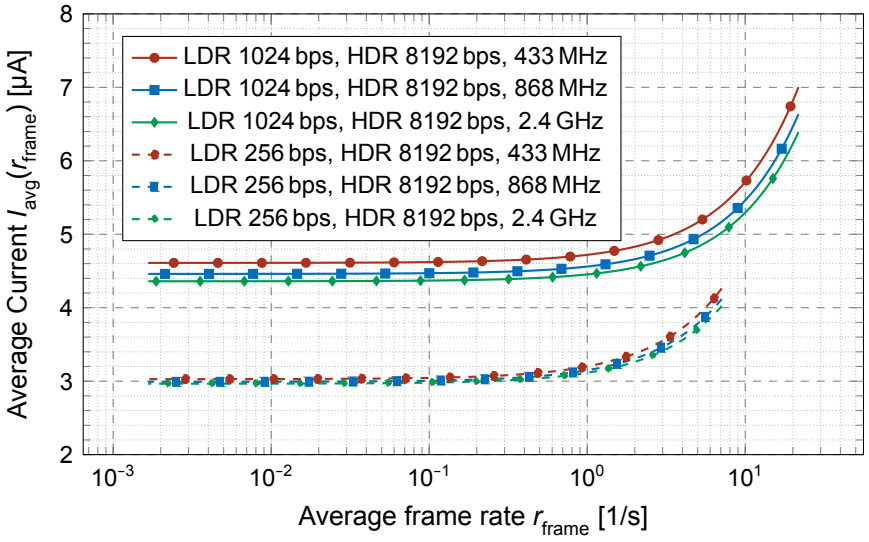


Figure 8: Average current over frame rate, assuming 2 bytes receiver ID and 6 bytes data for FIFO buffer.

In the given example, if 8-byte messages are received only every 8 seconds on average or less frequently, the receiver's current consumption remains very close to the consumption of listening for wake-up events according to tables 6 and 7. The maximum packet rates in this example result at 7.15 packets per second and 21.74 packets per seconds for the given data rate combinations and payload, assuming T_{P1} = 1 ms.

It is not recommended to activate FDD reception mode (sec. 7.6) if transmission and reception of ID or payload data is generally not intended.

5.7 Power Up

The general use-case is to supply the RFicient® receiver from a single battery source while using the internal LDO to generate the core voltage VDDC (see section 5.2 for battery requirements). The minimum voltage at VDDIO for the receiver to operate is 1.8 V. Common commercially available lithium coin cells are discharged to 10 % of their initial charge at 2.5 V (e.g. CR2032). Internal power-up check routines are executed upon connection of the supply. As soon as the VDDIO voltage is greater than 1.8 V, the LDO starts operating (chip default). For this, the external decoupling capacitances at VDDC must be connected at the VDDC pin according to figure 5.

Depending on the application the user may want to achieve a CLK32_XI clock signal at current consumptions below those provided by the RFicient® IC's integrated clock generator. In this case the CLK32_XI signal can be supplied by an external clock source with extremely low current consumption (e.g. $I_{avg,clock} \leq 100$ nA). The internal clock generator may be disabled by setting bit 0 in register XTAL_OSC_ENA (address 0x73) to 0.

The flow chart in figure 9 illustrates the power-up routine and necessary steps. The internal clock

[2]Comprised of 2 bytes for the receiver ID (ID match) and 6 bytes for the FIFO buffer.

oscillator starts operating automatically, if an external crystal is connected (cf. section 5.1).

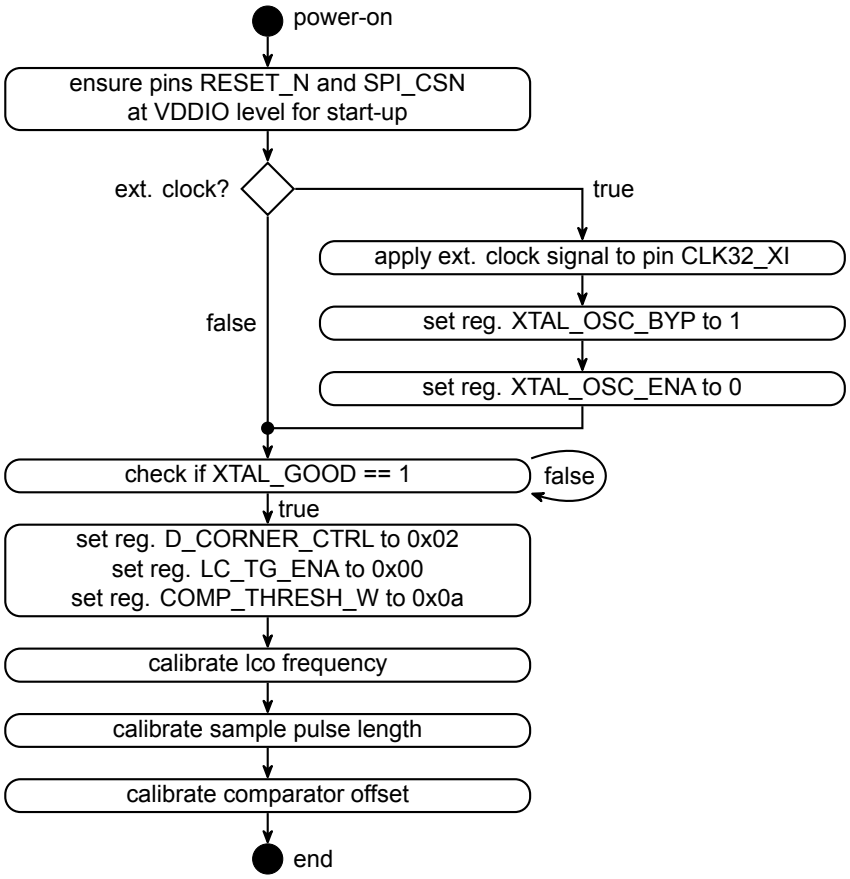


Figure 9: Flow chart of power-up routine.

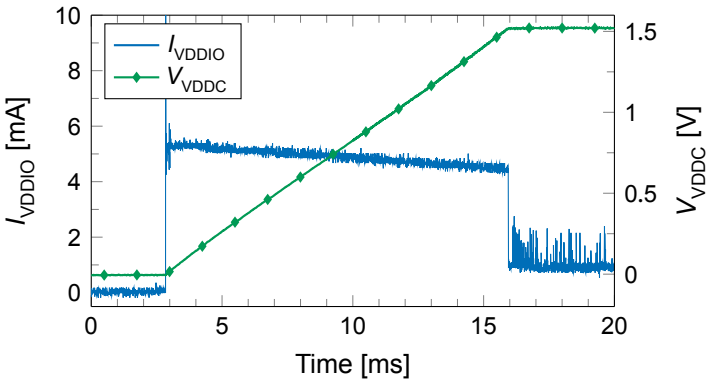


Figure 10: Transient current consumption during power ramp-up

⚠ On power-up ensure that all digital input pins are non-floating. The device does not use internal pull resistors. Floating inputs can lead to undefined behaviour and be potentially harmful to the device.

After power-up of the receiver, the user has to check stability of the clock source by verifying if register XTAL_GOOD is set to 1 by the chip. This is mandatory for proper receiver operation. Only then calibrations and reception of RF messages can be performed. XTAL_GOOD typically transitions from 0 to 1 approximately 0.5 s after the oscillation has started (room temperature).

Figure 10 shows a typical measurement of the current drawn from a battery at power-up for the application circuit as in figure 5. The voltage V_{VDDC} is ramped up as as C6 and C7 are charged with

≈ 5 mA.

⚠ It is *mandatory* to *execute all built-in calibration methods* (cf. section 7.3) to achieve optimum sensitivity and current consumption after power-up. Please ensure the proper order of calibration methods indicated in the power-up routine given in figure 9.

5.7.1 Power Supply PCB Recommendations

A good power supply layout is required to achieve the specified performance. The blocking capacitors, described in table 10, must be placed near the corresponding power pad, thus avoiding undesirable inductances in the power supply path. Figure 11 shows a possible arrangement of the blocking capacitors in the layout. A good ground connection must also be ensured, especially on the chip exposed pad. Ideally this should be solid connected to the board ground plane, which also represents the RF feed return path.

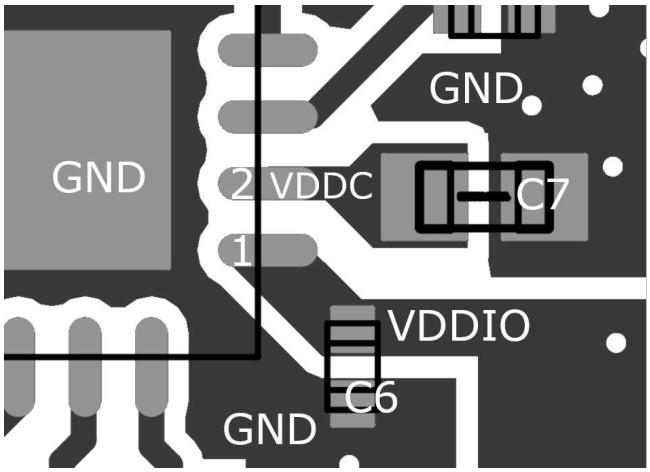


Figure 11: Example PCB layout with power supply blocking capacitors C6 and C7.

5.8 Transmitter Requirements

In order to receive wake-up telegrams, transmitters must be set to pulse modulation (OOK), ensuring a TX power level for the low level (data zero) well below −60 dBm, preferably at −80 dBm.

⚠ The TX data rate f_{TX} *must* be set at a 1 % higher value than the receivers sampling rate according to

$$f_{TX} = 1.01 \frac{32{,}768\,\text{Hz}}{2^{NFA}},$$

where NFA is the decimal value contained in registers 0x00 to 0x05, defining the sampling rate with respect to preamble listening (LDR), data transfer of ID and FDD data (HDR) and frequency band. (see sections 5.6 and 7.2.)

To ensure minimum wake-up error rate (WER ≤ 10^{-3}) at the receiver's sensitivity level, a modulation bandwidth of 500 kHz is recommended on the TX signal at the maximum sampling rate of 32,768 Hz. This corresponds to a rise time of the baseband signal of 2 µs from 10 % to 90 %. At a modulation bandwidth of 250 kHz the receiver's sensitivity is reduced by 1 dB for a required wake-up error rate WER = 10^{-3}. For reduced sampling and tx data rates, the modulation bandwidth can be reduced according to the selected factor NFA.

6 Receiver Control

6.1 The 3-Wire SPI Interface

The RFicient® receiver can be accessed by the user with a 3-wire SPI protocol compliant interface, where the RFicient® IC acts as slave. There is read and write access depending on the register type according to the read/write-direction mentioned in table 31.

Each SPI access is initiated by falling edge and finished by rising edge at the chip select SPI_CS_N pin. SPI_SIO acts as a bi-directional input and output for address and data values. Any transaction starts with a header byte comprised of one bit to decide read (HI) or write (LO) operation and a 7-bit address A6 to A0, selecting the register according to table 31.

Address and data bits on the SPI_SIO line must be stable with the positive edge of the clock SPI_CLK, ensuring the setup and hold times t_{set} and t_{hld} and a maximum clock frequency of 10 MHz, as indicated in figure 12 with bounding values given in table 17.

In write mode the header byte must be followed by a data byte, containing the data to be written to the register. For read access, the SPI_SIO pin changes its data direction after header byte transmission and outputs the addressed register data in 8 SPI_CLK clocks.

An overview of the addressable register set can be found in table 31.

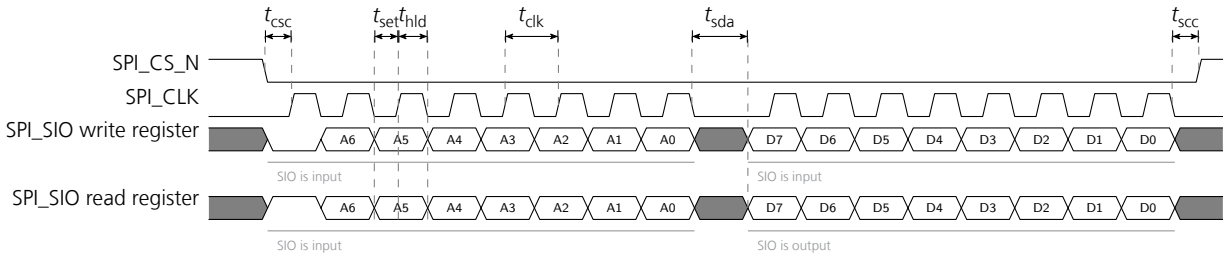


Figure 12: Timing Diagram for SPI Read/Write Operation.

Parameter	Description	Min.	Unit
t_{clk}	SPI_CLK period	100	ns
t_{csc}	Time SPI_CS_N falling edge to first SPI_CLK rising edge	5	ns
t_{set}	SPI_SIO setup, data must be stable before SPI_CLK rising edge	15	ns
t_{hld}	SPI_SIO data hold	5	ns
t_{sda}	SPI_SIO data setup	10	ns
t_{scc}	Last SPI_CLK falling edge to SPI_CS_N rising edge	5	ns

Table 17: SPI Timing Requirements.

6.2 Connecting to a 4-wire SPI master

The RFicient® receiver's 3-wire SPI interface can be connected to any 4-wire-interface using a resistor R_s as shown in figure 13. Assuming pad capacitance of 2 pF and a maximum SPI clock-speed of 10 MHz resistor R_s should have a value of 3 kΩ. Hence, a current of approximately 1 mA will flow from VDDIO during read operation at VDDIO voltage of 3 V.

⚠ Set the master's MOSI port to a LO state, when there is no SPI communication, to ensure no static current flow!

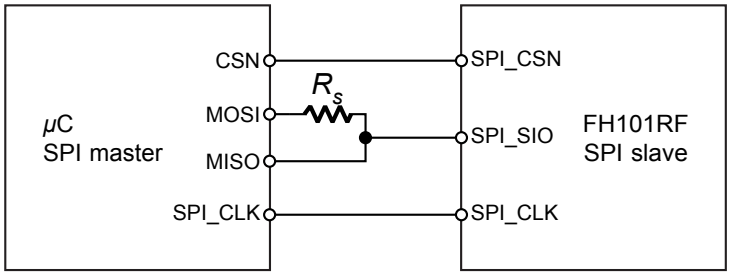


Figure 13: Connecting the 3-wire FH101RF slave to a 4-wire SPI master.

7 Register Description

7.1 RF Band and Branch Control

Register 0x24 BAND_BRANCH_CTRL

Branch Control Bits 2:0 select the RX branches for various RF-sensitivity levels. Writing 1 into bit 0 activates the reception branch for detection of weak RF signals with highest sensitivity (see table 8). Setting bit 1 to one, activates the reception branch for “medium” RF signals (at least 8 dB stronger than weak), bit 2 for strong RF signals (e.g. very short distance, at least 16 dB stronger than weak). Chip default is $(111)_2$, i.e. all RX-branches are activated. This ensures better robustness against in-band interferer signals. The current consumption is slightly affected by the number of activated branches. Branch activation also allows coarse assessment of the strength of received wake-up-message levels, by evaluating register 0x2B (cf. section 7.5).

Band Control Bits 6:4 select the desired RF frequency bands for wake-up reception. Note: Simultaneous reception at two or three frequency bands is possible! Bit 4 selects the 433-MHz band, bit 5 selects the 868-MHz band, bit 6 selects the 2.4-GHz band. Note: The number of selected frequency bands strongly determines the current consumption of the receiver (cf. tables 6 and 7).

BAND_BRANCH_CTRL<6:4>	2400 MHz	868 MHz	433 MHz	Comment
0b000	–	–	–	no band selected
0b001	–	–	active	mono-band
0b010	–	active	–	mono-band
0b011	–	active	active	dual-band
0b100	active	–	–	mono-band
0b101	active	–	active	dual-band
0b110	active	active	–	dual-band
0b111	active	active	active	tri-band (chip default)

Table 18: Modes for multi-band operation.

7.2 Sampling Modes

Registers 0x00 to 0x05 select the sampling rates of the receiver for the three receiver-bands in the low-data-rate (LDR) and high-data-rate (HDR) modes respectively. Table 19 shows the effect the NFA settings one each of these registers. Refer to section 5.6 for a description of the wake-up protocol, with ID match (IDM) and fast data decoder (FDD).

Registers denoted with the suffix *_SLOW set the data-rate for the LDR-only mode or the preamble. Registers denoted *_FAST set the data-rate for the high-data-rate sampling of FDD- or IDM-data accordingly.

In dual-band or tri-band mode (cf. section 7.1) the user can check which data rates are actually effective. See registers 0x6C to 0x6E (ACTUAL_NFA) and 0x6F (ACTUAL_BANDSELECT).

For ultra-low power operation achieving lowest current consumptions, the user should choose NFA<band>_SLOW = 0x07 (cf. tables 6 and 7). Hence, the 32-bit wake-up sequence has a duration of 125 ms.

NFAxxx_SLOW/FAST<2:0> [binary]	Sample Rate [Hz]	Code-Sequence-Duration [ms]	Comment
0b000	32,768	0.977	fastest for mono-band
0b001	16,384	1.953	fastest for dual-band, fastest for 868-MHz band in tri-band mode
0b010	8192	3.906	fastest for 433-MHz and 2.4-GHz band in tri-band mode
0b0b011	4096	7.813	–
0b100	2048	15.625	–
0b101	1024	31.250	typical
0b110	512	62.500	–
0b111	256	125.000	slowest

Table 19: Sampling modes for various NFA settings.

Register 0x00: NFA433_SLOW

Bits 2:0: NFA433_SLOW set the sample-rate for preamble-listening (LDR-mode with FDD/IDM enabled) or single-sequence wake-up (FDD disabled) in the 433-MHz band.

Register 0x01: NFA433_FAST

Bits 2:0: NFA433_FAST set the fast sample rate (HDR) for fast RX operation (enabled FDD mode) for the 433-MHz band.

Register 0x02: NFA868_SLOW

Bits 2:0: NFA868_SLOW set the sample-rate for preamble-listening (LDR-mode with FDD/IDM enabled) or single-sequence wake-up (FDD disabled) in the 868-MHz band.

Register 0x03: NFA868_FAST

Bits 2:0: NFA868_FAST set the fast sample rate (HDR) for fast RX operation (enabled FDD mode) for the 868-MHz band.

Register 0x04: NFA2G4_SLOW

Bits 2:0: NFA2G4_SLOW set the sample-rate for preamble-listening (LDR-mode with FDD/IDM enabled) or single-sequence wake-up (FDD disabled) in the 2.4-GHz band.

Register 0x05: NFA2G4_FAST

Bits 2:0: NF2G4_FAST set the fast sample rate (HDR) for fast RX operation (enabled FDD mode) for the 2.4-GHz band.

7.3 Calibration Control

Internal automatic calibration-algorithms compensate for device-to-device variation and temperature dependent sensitivity-degradation of the receiver. Refer to the instructions and register-descriptions in the following subsections to execute these calibration-algorithms.

Register 0x06 CALIB_STATUS

Bit 0 (CAL_IN_PROG) is 0 if no calibration is in progress and is 1 during an ongoing calibration calibration. The receiver automatically sets and clears this bit during calibration. The user can check with this bit, if calibration has completed. Bits 3:1 show which calibration is active.

Register 0x07 CALIB_CTRL

Bits 3:1 select each calibration methods LCO_CAL, SPG_CAL and OFFSET_CAL, described in the following subsections. If the user sets bit 0 (CAL_START) to “1”, the selected calibration methods are initiated.

⚠ It is required that only one calibration method is selected and executed at one time. Please ensure the proper order of calibration methods according to figure 9.

7.3.1 Comparator Calibration

The comparator calibration (OFFSET_CAL) compensates internal process related offset voltages. It is required to execute the comparator calibration after start-up and periodically thereafter, depending on the application. This helps to ensure RF sensitivity, as shown in section 2.4, figure 3. Refer to the calibration flow diagram in figure 14 on how to execute the comparator calibration. See section 7.4 for recommendations on calibration frequency and expected additional current consumption.

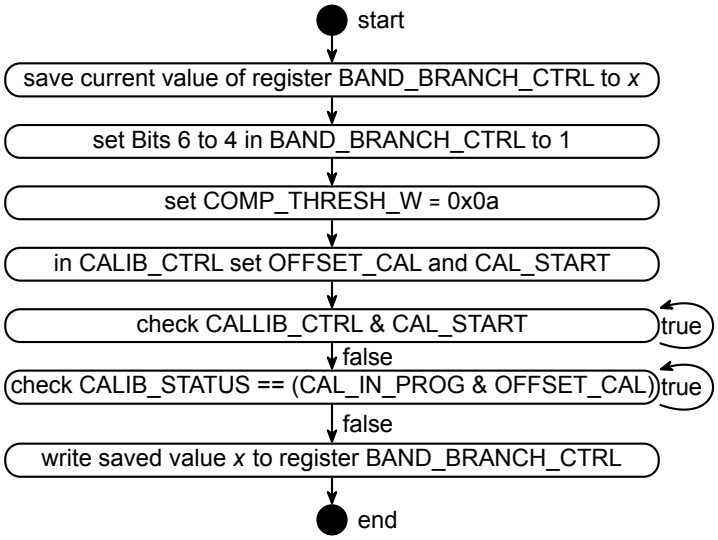


Figure 14: Comparator calibration routine flow chart.

7.3.2 Oscillator Calibration

The local oscillator calibration (LCO_CAL) adjusts the internal local oscillator (LO) for the appropriate radio-frequency for reception of wireless signals. The calibration operates only on selected frequency bands (cf. BAND_BRANCH_CTRL). It is mandatory to start the oscillator calibration after start-up for the desired frequency bands.

Refer to the calibration flow diagram in figure 15 on how to execute the oscillator calibration. It is

recommended to leave the target values N_LCO_TARGET_<band> at default values for use with the default RF frequencies f_{RF} at 433 MHz, 868 MHz and 2480 MHz respectively. The default values yield LO frequencies $f_{LO,<band>}$ at 473 MHz, 908 MHz and 2524 MHz and a resulting optimum intermediate frequency f_{IF} = 40 MHz for all bands.

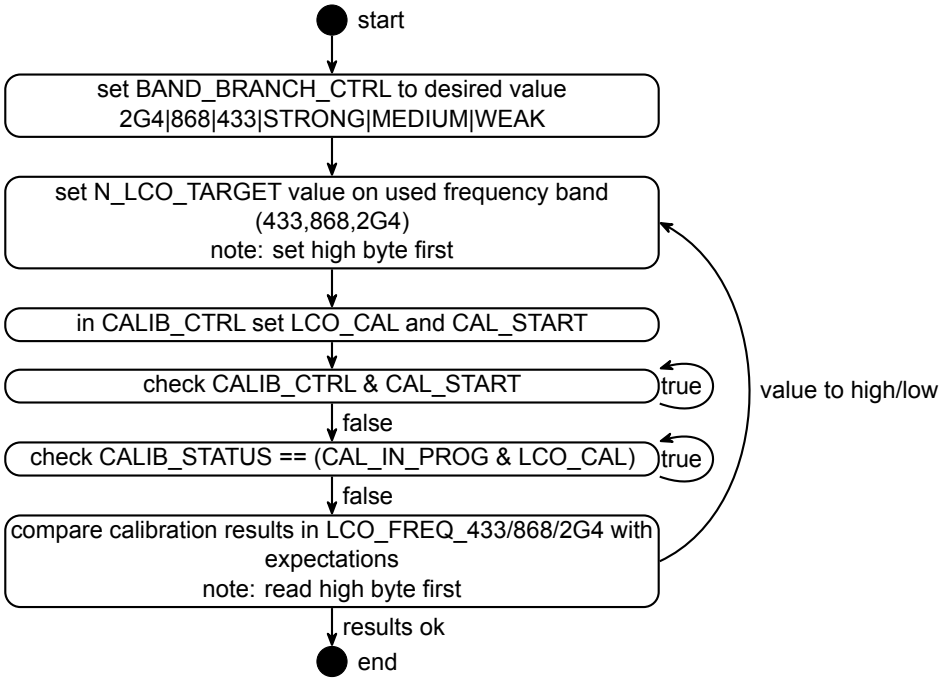


Figure 15: Oscillator calibration routine flow chart.

RF expert users may adjust f_{RF} and f_{LO} depending on local interferer scenarios, ensuring that $f_{IF} = |f_{RF} - f_{LO}|$ lies between corner frequencies 30 MHz and 50 MHz with the sensitivity optimum at f_{IF} = 40 MHz. At either corner frequencies 1 dB sensitivity degradation is to be expected. Operation at f_{RF} = 915 MHz is possible via pin 11[3] (RFIN_868), by choosing N_LCO_TARGET_868 = 3643 and $f_{LO,868}$ = 955 MHz.

Note: At the sub-1-GHz bands at f_{RF} at 433 MHz or 868 MHz the LO frequency adjustment is only available for high-side injection ($f_{LO} > f_{RF}$). For an RF frequency of 915 MHz both high-side and low-side injection are available. Table 20 shows allowed target values for register values of N_LCO_TARGET_<band> for respective bands. Resulting LO target frequencies can be calculated from N_LCO_TARGET_<band> register values by

$$f_{LO,<band>} = \text{N\_LCO\_TARGET\_<band>} \times m \times 32{,}768\ \text{Hz}, \quad (3)$$

where the factor m assumes the values 4, 8 and 16 for the bands at 433 MHz, 868 MHz and 2400 MHz respectively. Using the evaluation kit, setting the RF frequencies in the user interface, automatically executes the LO calibration according to figure 15 using equation 3.

SRD band [MHz]	**LO frequency** [MHz]		**N_LCO_TARGET value**	
	Min	**Max**	**Min**	**Max**
433	433	510	3304	3891
868 / 915	860	980	3281	3738
2400	2350	2534	4482	4833

Table 20: Allowed values for registers and corresponding LO frequencies.

[3] In this case the SAW-filter and matching network from figure 5 do not apply.

The measured temperature drift of the local oscillator frequency for the three available SRD bands is given in table 21 in kHz per Kelvin. See section 7.4 for recommendations on calibration frequency and expected additional current consumption.

SRD band [MHz]	LO frequency temperature drift [kHz/K]
433	67
868 / 915	136
2400	327

Table 21: Measured LO drift with temperature.

Register 0x0B N_LCO_TARGET_433<15:8>,
Register 0x0C N_LCO_TARGET_433<7:0>,
Register 0x0D N_LCO_TARGET_868<15:8>,
Register 0x0E N_LCO_TARGET_868<7:0>,
Register 0x0F N_LCO_TARGET_2G4<15:8>,
Register 0x10 N_LCO_TARGET_2G4<7:0>

These register values are used to set the local oscillator frequency. Constraints from table 20 apply.

Register 0x14 LCO_FREQ_433<15:8>,
Register 0x15 LCO_FREQ_433<7:0>,
Register 0x16 LCO_FREQ_868<15:8>,
Register 0x17 LCO_FREQ_868<7:0>,
Register 0x18 LCO_FREQ_2G4<15:8>,
Register 0x19 LCO_FREQ_2G4<7:0>

These read-only registers are reserved for internal automatic frequency adjustment and are used to check internal frequencies. Please read the registers in the given order from 0x14 to 0x19.

7.3.3 Sample Pulse Calibration

The sample pulse calibration adjusts internal time references. It is recommended to execute the sample pulse calibration after start-up. Regular pulse calibrations during operation are not necessary. Refer to the calibration flow diagram in figure 16 on how to execute the sample pulse calibration.

⚠ For optimal current consumption the register N_SPG_TARGET (address 0x09) needs to be set to the non-default value 0x46.

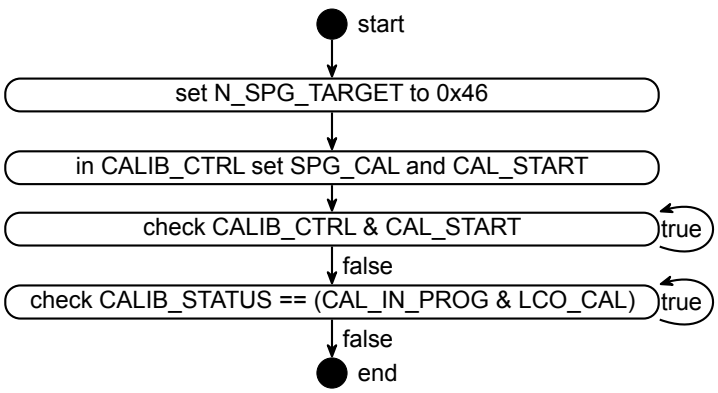
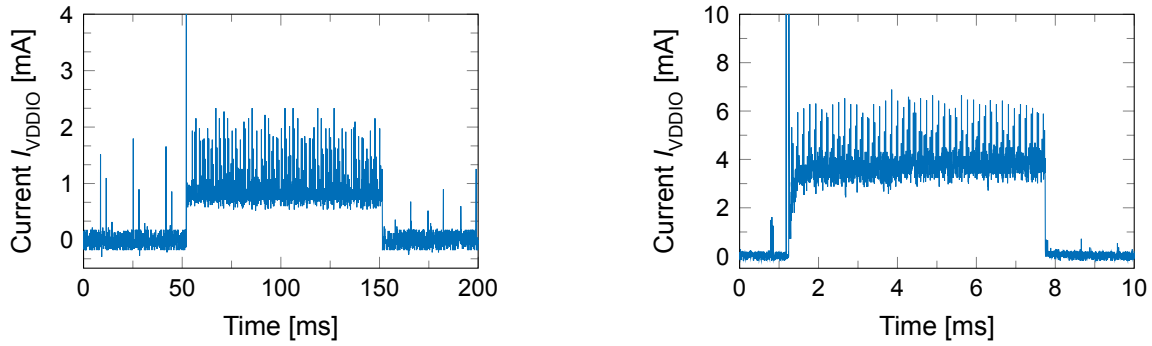


Figure 16: Sample pulse calibration routine flow chart.

7.4 Calibration Current Consumption and Recommended Calibration Frequency

For battery lifetime estimations depending on calibration frequency, figures 17a and 17b show the transient current consumption and duration while comparator and oscillator calibrations are executed. The calibration durations are approximately 100 ms for comparator calibration and 7 ms for oscillator calibration. Note: The receiver cannot receive wake-up messages during any calibration.

It is generally recommended to execute the comparator and oscillator calibrations at every change of 10 °C in ambient temperature. If no temperature data is available, calibrations should be executed in periodic time intervals, with an interval duration depending on the application and expected temperature changes.



(a) Comparator calibration current.

(b) Oscillator calibration current.

Figure 17: Transient current consumption during calibration.

In temperature-stable environments (e.g. heated and/or air-conditioned indoor environments) calibrations can be executed less often: e.g. every 60 minutes to 360 minutes, depending on current and battery-lifetime requirements. For convenience, table 22 lists the currents drawn at average oscillator and comparator calibration intervals, for each calibration method.

Calibration interval [min]	**Additional current drawn** [µA]	
	LO calibration	**Comparator calibration**
1.0	0.43	1.70
5.0	0.09	0.33
10.0	0.04	0.17
15.0	0.03	0.11
30.0	0.01	0.06
60.0	0.01	0.03

Table 22: Additional current drawn per calibration interval.

7.5 Wake Up Code Related Registers

Register 0x28 CODE_SELECT

A number of predefined bit sequences can be selected as correlation patterns to match either as “code A” or as “code B” according to the wake-up protocol described in section 5.6. In register 0x28 bits 3:0 define the index to select the pattern for the code A sequence, according to the indexed list in table 23. Bits 7:4 define the selection of the code B sequence accordingly. Selected chip defaults “mls A” and “mls B” for code A and code B, ensure best receiver sensitivity because of highest error tolerance.

Modulating the patterns onto the OOK telegram on transmitter side, MSBs have to be transmitted first.

Index	Binary 32-bit Sequence	Decimal Value	Name
0	0110 1010 1100 1101 0110 0111 0100 1111	1,791,846,223	mls A (default code A)
1	0110 1101 0011 1000 1001 0111 0111 0011	1,832,425,331	mls B (default code B)
2	0111 0010 0001 0011 0110 1010 0001 0110	1,913,874,966	mls C
3	0000 1101 1110 1100 1001 0101 1100 0111	233,608,647	mls D
4	0001 0101 0011 0010 1001 1000 1011 0000	355,637,424	mls A inv
5	0001 0010 1100 0111 0110 1000 1000 1100	315,058,316	mls B inv
6	0100 0010 0101 1001 1111 0001 1011 1010	1,113,190,842	m-sequence A
7	0100 0011 0010 0111 1101 1100 0101 0110	1,126,685,782	m-sequence B
8	0000 0000 0000 0000 0000 0000 0000 0000	–	31 zeros
9	0111 1111 1000 0000 0000 0000 0000 0000	–	8 ones
10	0111 1111 1111 1111 1000 0000 0000 0000	–	16 ones
11	0111 1111 1111 1111 1111 1111 1000 0000	–	24 ones
12	0111 1111 1111 1111 1111 1111 1111 1111	–	31 ones
13	0101 0101 0101 0101 0101 0101 0101 0101	–	0101 pattern
14	0110 0110 0110 0110 0110 0110 0110 0110	–	1100 pattern
15	0111 0001 1100 0111 0001 1100 0111 0001	–	111000 pattern

Table 23: Predefined 32-bit sequences for binary correlators “A” and “B”.

Register 0x29 KORREL_THRESH_A

Bits 4:0: KORREL_THRESH_A defines the correlator “A” threshold. Useful values are between 0x19 and 0x1E. Lower values of KORREL_TRESH correspond to more tolerated bit errors during reception of 32-bit code sequences. However, lowering KORREL_TRESH can increase the probability of false wake-up detections.

Register 0x2A KORREL_THRESH_B

Bits 4:0: KORREL_THRESH_B defines the correlator “A” threshold. Useful values are between 0x19 and 0x1E. Lower values of KORREL_TRESH correspond to more tolerated bit errors during reception of 32-bit code sequences. However, lowering KORREL_TRESH can increase the probability of false wake-up detections

Register 0x2B KORREL_STATE

Bits 2:0 indicate the receiver branch (cf. section 7.1) that had contributed for the Code A recognition. “Weak” (bit 0), “medium” (bit 1), “strong” (bit 2). These bits can indicate the reception level of the last wake-up sequence “A” that triggered above KORREL_THRESH_A.

Bits 5:3 indicate the receiver branch that had contributed for the Code B recognition. “Weak” (bit 0), “medium” (bit 1), “strong” (bit 2). These bits can indicate the reception level of the last wake-up sequence “B” that triggered above KORREL_THRESH_B.

Bits 7:6 indicate the frequency band for latest correlator A or B trigger. “00” means 433-MHz band, “01” means 868-MHz band, “10” means 2.4-GHz band. KORREL_STATE can be cleared by the user writing “1” into register 0x7C “KORREL_SV_CLEAR”. Thus, it gets cleared when the latest update of KORREL_STATE and KORREL_VAL took place.

Register 0x2C KORREL_VAL

Bits 3:0 indicates the correlator match level for the Code A recognition. These bits indicate the number of bit errors of the last wake-up sequence “A”. A value of 15 corresponds with no bit errors, a value of 0

corresponds with 15 bit errors. This register is only refreshed after a positive Code A match. Typically, KORREL_VAL is greater than 5.

Bits 7:4 indicates the correlator match level for the Code B recognition. These bits indicate the number of bit errors of the last wake-up sequence “B”. A value of 15 corresponds no bit errors, a value of 0 corresponds with 15 bit errors. This register is only refreshed after a positive Code B match. Typically, KORREL_VAL is greater than 5.

KORREL_VAL can be cleared by the user writing “1” into register 0x7C “KORREL_SV_CLEAR”. Thus, it gets cleared when the latest update of KORREL_STATE and KORREL_VAL took place.

Register 0x7C KORREL_SV_CLEAR

Writing „1“ into this register, clears the KORREL_STATE and the KORREL_VAL registers.

7.6 Data Reception Related Registers

Register 0x2D FDD_ENABLE

This register can be used to enable the fast data decoder (FDD) using bits 2 to 0 for the respective frequency bands, according to table 31. Enabling the fast data decoder (FDD) using bits 0:2, the RFicient® receiver interprets Code A sequences in slow operating mode as initiator for FDD packets. Incoming FDD bits are stored in the FIFO registers 0x2E:0x3F. Details on receiving data with the FDD and an ID are given in section 5.6.

Register 0x2E FDD_ACTIVE

This register stores the FDD mode (“1”: Fast Mode, “0”: Slow Mode) for each frequency band: Bit 2: 433 MHz band, bit 1:868 MHz band, bit 0: 2.4 GHz band. Only for read access.

Register 0x2F FO_QUIT

Writing ones into the FORCE_QUIT register, the user can force the receiver to quit fast mode immediately. This can be adjusted for each frequency band separately:

Bit 2: FO_QUIT_2G4: Setting this bit, the user can force the receiver to switch back to slow operation for the 2.4 GHz band.

Bit 1: FO_QUIT_868: Setting this bit, the user can force the receiver to switch back to slow operation for the 868 MHz band.

Bit 0: FO_QUIT_433: Setting this bit, the user can force the receiver to switch back to slow operation for the 433 MHz band.

Register 0x30 FDD_EXIT_COND

Bits 5:4: Indicates the 2-bit nibble for the 2.4 GHz band. Bits 3:2: Indicates the 2-bit nibble for the 868 MHz band. Bits 1:0: Indicates the 2-bit nibble for the 433 MHz band.

2 bit FDD_EXIT_COND nibble	Reason	Comment
0b00	RX resetted or FDD is disabled	initial entry
0b01	timeout	no FAST Code A or B received
0b10	ID match failed	wrong 16 bit ID
0b11	FO_QUIT was set	user forced slow mode

Table 24: Exit conditions for Fast Data Decoding.

7.7 Interrupt Related Registers

Register 0x31 IRQ_SELECT

The user can select among IRQ event types 0 to 7 according to table 13. Bit 7 (MSB) corresponds to event type 7 (Cyclic Timer Alarm), bit 0 (LSB) to type 0 (ID match). If more event types are desired, more bits need to be selected. If any of the selected event types occur, an IRQ signal will be generated. The event can be observed at the pins GPO1 or GPO2, if configured accordingly to table 15.

Register 0x32 IRQ_STATUS

If any of the selected IRQ event types (reg. 0x31) occur, an IRQ signal will be generated. This can be observed at the pins GPO1 or GPO2. In register 0x32, the occurred IRQ event types 0..7 are marked with set bits according to table 13. Register 0x32 is a read-only register. It can be cleared by access to register 0x33.

Example: If register 0x32 contains 0x49 $(01001001)_2$, the RTC Timer alarm has occurred, Code A or B have been detected and ID match was triggered.

Register 0x33 IRQ_CLR

If the user writes “1” bits into this register, the corresponding bit in register 0x32 will be cleared.

Example: If the IRQ status register 0x32 contains the value 0x49, a write access to IRQ_CLR (reg. 0x33) writing 0x48 causes cleared bits in reg. 0x32: The new content will be 0x01, as the LSB has not been cleared by register 0x33.

Note: Bits 4, 2 and 1 (FIFO-buffer filled) cannot be cleared. To clear the IRQ_STATUS bits 4, 2 and 1, the user must clear the FIFO buffer first by setting FIFO_COUNT to 0 (reg. 0x57, 0x58 or 0x59).

Register 0x34 IRQ_SET

By writing ones into this register, the user can set the corresponding status bit in the IRQ_STATUS register. Thus, IRQ events can be triggered for test purposes.

Example: Writing 0x41 $(01000001)_2$ into reg. 0x34 causes set bits for event type 6 (RTC) and event type 0 (ID match) in register 0x32 IRQ_STATUS.

7.7.1 IRQ Handling

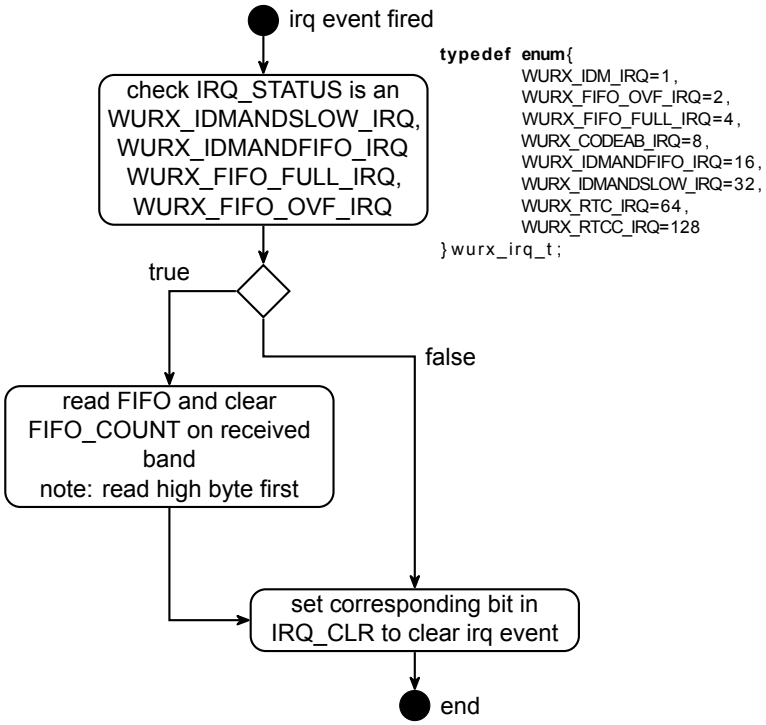


Figure 18: Flow chart for IRQ handle.

7.8 ID and Group-ID Related Registers

Register 0x38 IDM_CTRL

Bits 1:0 of this register select the type of ID which will be accepted by the receiver. The receiver can generally be addressed in three ways: individual wake-up, group wake-up or a broadcast call to wake-up all nodes. Use table 25 to set whether the receiver accepts only individual wake-up calls, individual or group-calls, only broadcast, or any one of the three ID types..

IDM_CTRL<1:0>	selected ID Match Method	Comment
0b00	only individual 16 bit ID	–
0b01	individual 16 bit ID or groupwise ID	–
0b10	only broadcast ID	–
0b11	individual 16 bit ID, groupwise ID, or broadcast ID	default

Table 25: Available modes for selective wake-up.

The individual 16 bit ID is set in registers 0x35 and 0x36. Chip default is 0x7DA8, which is 0111 1101 1010 1000 in binary. Mapping the selected code-symbols from table 23 to correlators A and B, the according RF OOK telegram to address ID 0x7DA8 should look like:

(slow) A (fast) ABBB BBAB BABA BAAA.

To group-ID constitutes as follows. The most significant 4 bit of the group ID are derived from the 4 MSBs of the individual 16 bit ID:

GROUP_ID<15:12> := ID<15:12>.

The residual 12 bit of the group ID are zero:

$$\text{GROUP\_ID<11:0>} := 0.$$

Group calls are transmitted similar as a 16 bit ID telegram.

Example for group 0x0B or 0b1011:

```
1011 0000 0000 0000
```

The RF OOK telegram should look like:

```
(slow) A (fast) BABB AAAA AAAA AAAA
```

The 16-bit broadcast ID is 0x032F or 0000 0011 0010 1111 binary and fixed for all RFicient® receivers. This can be used for network messages addressing all RX nodes. The broadcast ID cannot be changed. The RF OOK telegram should then look like:

```
(slow) A (fast) AAAA AABB AABA BBBB.
```

Register 0x39 IDM_CLR

Writing “1” into this register clears reg. 0x30 (FDD_EXIT_COND).

Register 0x3A IDM_BAND

This register indicates the frequency band for the latest ID Match event. Binary “00” means 433 MHz band, “01” means 868 MHz band, “10” means 2.4 GHz band.

Register 0x3B IDM_REASON

Bits 1:0 indicate the type of received selective wake-up message.

IDM_REASON<1:0>	Reason
0b00	–
0b01	individual ID
0b10	group ID
0b11	broadcast ID

Table 26: Types of incoming selective wake-up message.

7.9 Real Time Counter

Register 0x3C RTC_SELECT

Register values RTC_SELECT<4:0> allow for selection of the desired timer modes described in table 14. Each of the five bits enables or disables (active HI) its corresponding timer according to table 27. Arbitrary combinations are possible. The RTC timers can generate interrupt events, which are described in sections 5.3 and 7.7.

Register Bit	Controlled Timer	Description
RTC_SELECT<4>	CYCLTOP	cyclic counter
RTC_SELECT<3>	RTCLG1	long RTC counter #1
RTC_SELECT<2>	RTCLG0	long RTC counter #0
RTC_SELECT<1>	RTCSH1	short RTC counter #1
RTC_SELECT<0>	RTCSH0	short RTC counter #0

Table 27: RTC Timer Selection Scheme.

Register 0x3D RTC_STATUS

Values in RTC_STATUS<3:0> indicate occurrence of RTC events, according table 28. Note that only enabled RTC timers can generate RTC events that will trigger IRQ6. As long as one event is active (corresponding bit in RTC_STATUS is set), IRQ6 cannot be cleared.

Register Bit	Corresponding Timer
RTC_STATUS<3>	RTCLG1
RTC_STATUS<2>	RTCLG0
RTC_STATUS<1>	RTCSH1
RTC_STATUS<0>	RTCSH0

Table 28: RTC Timer Status Scheme.

Register 0x3E RTC_CLR

Writing ones into register RTC_CLR<3:0>, the user can clear the respective event entries in RTC_STATUS<3:0> according to table 29.

Register Bit	Cleared Bit
RTC_CLEAR<3>	RTC_STATUS<3>
RTC_CLEAR<2>	RTC_STATUS<2>
RTC_CLEAR<1>	RTC_STATUS<1>
RTC_CLEAR<0>	RTC_STATUS<0>

Table 29: RTC Clear Status Bits.

Register 0x3F RTCSH0_THRESH<15:8>, Register 0x40 RTCSH0_THRESH<7:0>

Upper byte RTCSH0_THRESH<15:8> is stored at address 0x3F, lower byte RTCSH0_THRESH<7:0> is stored at address 0x40. RTCSH0_THRESH defines the counter threshold when RTCSH0 will stop and trigger status transition in RTC_STATUS<0>.

Register 0x41 RTCSH1_THRESH<15:8>, Register 0x42 RTCSH1_THRESH<7:0>

Upper byte RTCSH1_THRESH<15:8> is stored at address 0x41, lower byte RTCSH1_THRESH<7:0> is stored at address 0x42. RTCSH1_THRESH defines the counter threshold when RTCSH1 will stop and trigger status transition in RTC_STATUS<1>.

Register 0x43 RTCLG0_THRESH<39:32>, Register 0x44 RTCLG0_THRESH<31:24>, Register 0x45 RTCLG0_THRESH<23:16>, Register 0x46 RTCLG0_THRESH<15:8>, Register 0x47 RTCLG0_THRESH<7:0>:

RTCLG0_THRESH is a 40 bit register. Upper byte RTCLG0_THRESH<39:32> is stored at address 0x43, 2nd byte RTCLG0_THRESH<31:24> is stored at address 0x44. 3rd byte RTCLG0_THRESH<23:16> is stored at address 0x45. 4th byte RTCLG0_THRESH<15:8> is stored at address 0x46. 5th byte RTCLG0_THRESH<7:0> is stored at address 0x47. RTCLG0_THRESH<39:0> defines the counter threshold when RTCLG0 will stop and trigger status transition in RTC_STATUS<2>.

Register 0x48 RTCLG1_THRESH<39:32>,
Register 0x49 RTCLG1_THRESH<31:24>,
Register 0x4A RTCLG1_THRESH<23:16>,
Register 0x4B RTCLG1_THRESH<15:8>,
Register 0x4C RTCLG1_THRESH<7:0>:

RTCLG1_THRESH is a 40 bit register. Upper byte RTCLG1_THRESH<39:32> is stored at address 0x48, 2nd byte RTCLG1_THRESH<31:24> is stored at address 0x49. 3rd byte RTCLG1_THRESH<23:16> is stored at address 0x4A. 4th byte RTCLG1_THRESH<15:8> is stored at address 0x4B. 5th byte RTCLG1_THRESH<7:0> is stored at address 0x4C. RTCLG1_THRESH defines the counter threshold when RTCLG1 will stop and trigger status transition in RTC_STATUS<3>.

Register 0x4D CYCLPRESC

The chip provides periodic alarms derived from the system clock (readable in register CNTR40) divided by the CYCLPRESC as the divisor, with 1 ≤ CYCLPRESC ≤ 255. Thus, a maximum alarm period of 8 min and 29.9922 s (i.e. 16,711,425 clock cycles) can be adjusted.

Register 0x4E CYCLTOP<15:8>, Register 0x4F CYCLTOP<7:0>:

The value in register CYCLTOP<15:0> (address 0x4E, 0x4F) defines the maximum cyclic counter value. Having reached this values, the cyclic counter CYCLCOUNT is automatically set to zero again. Thus, the 16 bit counter CYCLCOUNT runs repetitively from 0 to CYCLTOP. Reaching CYCLTOP, IRQ event 7 can be triggered if properly enabled (see sections 5.3 and 7.7).

Register 0x50 CNTR40<39:32>,
Register 0x51 CNTR40<31:24>,
Register 0x52 CNTR40<32:16>,
Register 0x53 CNTR40<15:8>,
Register 0x54 CNTR40<7:0>:

CNTR40 is a 40 bit register that represents the internal system clock counter (based on 32,768 Hz) since last reset. This counter will overflow after 33,554,432 s (i.e. 1 a, 23 d, 8 h, 40 m, 32 s or 2^{40} – 1 clock cycles). Hence, this built-in clock offers unique time stamps for one full year. Address 0x50 contains CNTR40<39:32>, address 0x51 contains CNTR40<31:24>, address 0x52 contains CNTR40<23:16>, address 0x53 contains CNTR40<15:8>, address 0x54 contains CNTR40<7:0>. It is mandatory to read the full register CNTR40<39:0> in the order 0x50 to 0x54 en bloc. This is a read-only register.

Register 0x55 CNTR40_CLR

Writing ”1” into this register, the CNTR40 will reset the counter. Manually setting the register to ”0” afterwards is mandatory.

7.10 FIFO Databuffer Control

Register 0x56 FIFO_LENGTH

Addressing register 0x56 FIFO_LENGTH<5:0>, the user can choose the length of the FIFO buffer for each frequency band, according to table 30.

Bits FIFO_LENGTH<1:0> define the length of the FIFO buffers for incoming fast data bits in FDD mode for the 433 MHz frequency band. Default is 16 bit. Bits FIFO_LENGTH<3:2> define the length the FIFO buffers for incoming fast data bits in FDD mode for the 868 MHz frequency band. Default is 24 bit. Bits FIFO_LENGTH<5:4> define the length of the FIFO buffers for incoming fast data bits in FDD mode for the 2.4 GHz frequency band. Default is 24 bit.

Register-value	FIFO length [bit]
0b00	16
0b01	24
0b10	32
0b11	40

Table 30: Available FIFO buffer length settings.

Register 0x57 FIFO_COUNT_433

Bits 5:0 indicate the number of received FDD bits in the FIFO buffer for the 433 MHz band. The user can write “0” in this register in order to clear the FIFO buffer.

Register 0x58 FIFO_COUNT_868

Bits 5:0 indicate the number of received FDD bits in the FIFO buffer for the 868 MHz band. The user can write “0” in this register in order to clear the FIFO buffer.

Register 0x59 FIFO_COUNT_2G4

Bits 5:0 indicate the number of received FDD bits in the FIFO buffer for the 2.4 GHz band. The user can write “0” in this register in order to clear the FIFO buffer.

Register 0x5A RX_FIFO_5_433,
Register 0x5B RX_FIFO_4_433,
Register 0x5C RX_FIFO_3_433,
Register 0x5D RX_FIFO_2_433,
Register 0x5E RX_FIFO_1_433,
Register 0x5F RX_FIFO_0_433:

These 8 bit registers form the FIFO buffer for the 433 MHz band. Register 0x5A is filled first.

Register 0x60 RX_FIFO_5_868,
Register 0x61 RX_FIFO_4_868,
Register 0x62 RX_FIFO_3_868,
Register 0x63 RX_FIFO_2_868,
Register 0x64 RX_FIFO_1_868,
Register 0x65 RX_FIFO_0_868:

These 8 bit registers form the FIFO buffer for the 868 MHz band. Register 0x60 is filled first.

Register 0x66 RX_FIFO_5_2G4,
Register 0x67 RX_FIFO_4_2G4,
Register 0x68 RX_FIFO_3_2G4,
Register 0x69 RX_FIFO_2_2G4,
Register 0x6A RX_FIFO_1_2G4,
Register 0x6B RX_FIFO_0_2G4:

These 8 bit registers form the FIFO buffer for the 2.4 GHz band. Register 0x66 is filled first.

7.11 Sampling Rate

Register 0x6C ACTUAL_NFA_433

This register contains the actual NFA value that is currently valid for 433 MHz data reception.

Register 0x6D ACTUAL_NFA_868

This register contains the actual NFA value that is currently valid for 868 MHz data reception.

Register 0x6E ACTUAL_NFA_2G4

This register contains the actual NFA value that is currently valid for 2.4 GHz data reception.

Register 0x6F ACTUAL_BANDSELECT

This 3 bit register contains the actual selected frequency bands that are currently used. Bit 2: indicates 2.4 GHz operation, Bit 1: indicates 868 MHz operation, Bit 0: indicates 433 MHz operation.

7.12 General Purpose Registers

Register 0x71 GENPURP_1

8 bit register free to use for read/write access.

7.13 On-Board Clock Oscillator & LDO Control

The system clock of 32,768 Hz determines the receivers sampling rate. External clock signal or internal clock-generator with external 2-pin crystal can be selected with the following register settings. Cf. sections 4 and 5.7 for more information.

Register 0x73 XTAL_OSC_ENA

1 bit register that enables the built-in crystal oscillator driving a 2-pin crystal device. Default: “1”.

Register 0x74 LDO_XTAL_CTRL

Bit 3, XTAL_OSC_BYP: Used for selecting an external system clock source that is applied to pin CLK32_XI. In this case, XTAL_OSC_BYP should be “1”. Set this, if a 2-pin crystal will not be used.

Bit 5, LDO_ENA_N: Used to deactivate the internal LDO for VDDC voltage generation. If set to 1, an external VDDC source must be supplied.

⚠ Bits 2:0: Reserved, do not change!

Register 0x77 XTAL_GOOD

This is a 1-bit read-only register. It value is 1 if the crystal oscillator has detected a stable system clock signal.

7.14 General Purpose Output Control

Register 0x75 MUX_D_OUT_SEL

The RFicient® receiver offers numerous internal signals that can be selected and provided at two output pins GPO1 and GPO2. Writing register 0x75, the user can choose according to table 15.

7.15 Comparator Threshold Control

Register 0x78 COMP_THRESH_W

Set this register to value 0xa before executing the comparator calibration (Sec. 7.3.1).

7.16 Chip Version

Register 0x7F VERSION

This is a read-only 8 bit register, that contains a version byte. Currently: 0x41.

Adress	Registername	Default Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0x00	NFA433_SLOW	0x05	--	--	--	--	--	NFA433_SLOW<2>	NFA433_SLOW<1>	NFA433_SLOW<0>	write
0x01	NFA433_FAST	0x00	--	--	--	--	--	NFA433_FAST<2>	NFA433_FAST<1>	NFA433_FAST<0>	write
0x02	NFA868_SLOW	0x05	--	--	--	--	--	NFA868_SLOW<2>	NFA868_SLOW<1>	NFA868_SLOW<0>	write
0x03	NFA868_FAST	0x00	--	--	--	--	--	NFA868_FAST<2>	NFA868_FAST<1>	NFA868_FAST<0>	write
0x04	NFA2G4_SLOW	0x05	--	--	--	--	--	NFA2G4_SLOW<2>	NFA2G4_SLOW<1>	NFA2G4_SLOW<0>	write
0x05	NFA2G4_FAST	0x00	--	--	--	--	--	NFA2G4_FAST<2>	NFA2G4_FAST<1>	NFA2G4_FAST<0>	write
0x06	CALIB_STATUS	0x00	--	--	--	--	OFFSET_CAL_IN_PROG	SPG_CAL_IN_PROG	LCO_CAL_IN_PROG	CAL_IN_PROG	read
0x07	CALIB_CTRL	0x0E	--	--	--	--	OFFSET_CAL	SPG_CAL	LCO_CAL	CAL_START	r/w
0x09	N_SPG_TARGET	0x31	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x0B	N_LCO_TARGET_433	0x0E	--	--	--	<12>	<11>	<10>	<9>	<8>	write
0x0C	N_LCO_TARGET_433	0x20	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x0D	N_LCO_TARGET_868	0x0D	--	--	--	<12>	<11>	<10>	<9>	<8>	write
0x0E	N_LCO_TARGET_868	0x87	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x0F	N_LCO_TARGET_2G4	0x12	--	--	--	<12>	<11>	<10>	<9>	<8>	write
0x10	N_LCO_TARGET_2G4	0xCE	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x14	LCO_FREQ_433	0x00	--	--	--	<12>	<11>	<10>	<9>	<8>	read
0x15	LCO_FREQ_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x16	LCO_FREQ_868	0x00	--	--	--	<12>	<11>	<10>	<9>	<8>	read
0x17	LCO_FREQ_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x18	LCO_FREQ_2G4	0x00	--	--	--	<12>	<11>	<10>	<9>	<8>	read
0x19	LCO_FREQ_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x23	D_CORNER_CTRL	0x00	--	--	CRN_S_ENA_SPG	CRN_F_ENA_SPG	CRN_S_ENA_MUXMIX	CRN_F_ENA_MUXMIX	CRN_S_ENA_LCO	CRN_F_ENA_LCO	write
0x24	BAND_BRANCH_CTRL	0x77	--	2G4	868	433	--	STRONG	MEDIUM	WEAK	write
0x28	CODE_SELECT	0x10	CODE_B<3>	CODE_B<2>	CODE_B<1>	CODE_B<0>	CODE_A<3>	CODE_A<2>	CODE_A<1>	CODE_A<0>	write
0x29	KORREL_THRESH_A	0x1A	--	--	--	<4>	<3>	<2>	<1>	<0>	r/w
0x2A	KORREL_THRESH_B	0x1A	--	--	--	<4>	<3>	<2>	<1>	<0>	r/w
0x2B	KORREL_STATE	0xC0	BAND<1>	BAND<0>	B_STRONG	B_MEDIUM	B_WEAK	A_STRONG	A_MEDIUM	A_WEAK	read
0x2C	KORREL_VAL	0x00	KORREL_VAL_B<3>	KORREL_VAL_B<2>	KORREL_VAL_B<1>	KORREL_VAL_B<0>	KORREL_VAL_A<3>	KORREL_VAL_A<2>	KORREL_VAL_A<1>	KORREL_VAL_A<0>	read
0x2D	FDD_ENABLE	0x07	--	--	--	--	--	FDD_2G4	FDD_868	FDD_433	write
0x2E	FDD_ACTIVE	0x00	--	--	--	--	--	FDD_ACTIVE_433	FDD_ACTIVE_868	FDD_ACTIVE_2G4	read
0x2F	FO_QUIT	0x00	--	--	--	--	--	FO_QUIT_2G4	FO_QUIT_868	FO_QUIT_433	write
0x30	FDD_EXIT_COND	0x00	--	--	<5>	<4>	<3>	<2>	<1>	<0>	read
0x31	IRQ_SELECT	0x01	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x32	IRQ_STATUS	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x33	IRQ_CLR	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x34	IRQ_SET	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x35	ID_HI	0x7D	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x36	ID_LO	0xA8	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x37	IDM_ENABLE	0x07	--	--	--	--	--	IDM_2G4	IDM_868	IDM_433	write
0x38	IDM_CTRL	0x00	--	--	--	--	--	--	IDM_CTRL<1>	IDM_CTRL<0>	write
0x39	IDM_CLR	0x00	--	--	--	--	--	--	--	IDM_CLR_STATUS	write
0x3A	IDM_BAND	0x03	--	--	--	--	--	--	IDM_BAND<1>	IDM_BAND<0>	read
0x3B	IDM_REASON	0x00	--	--	--	--	--	--	IDM_REASON<1>	IDM_REASON<0>	read
0x3C	RTC_SELECT	0x00	--	--	--	<4>	<3>	<2>	<1>	<0>	write
0x3D	RTC_STATUS	0x00	--	--	--	--	<3>	<2>	<1>	<0>	read
0x3E	RTC_CLR	0x00	--	--	--	--	<3>	<2>	<1>	<0>	write
0x3F	RTCSH0_THRESH	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	write
0x40	RTCSH0_THRESH	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x41	RTCSH1_THRESH	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	write
0x42	RTCSH1_THRESH	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x43	RTCLG0_THRESH	0x00	<39>	<38>	<37>	<36>	<35>	<34>	<33	<32>	write

Continued on next page...

Table 31: Register Set.

0x44	RTCLG0_THRESH	0x00	<31>	<30>	<29>	<28>	<27>	<26>	<25>	<24>	write
0x45	RTCLG0_THRESH	0x00	<23>	<22>	<21>	<20>	<19>	<18>	<17>	<16>	write
0x46	RTCLG0_THRESH	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	write
0x47	RTCLG0_THRESH	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x48	RTCLG1_THRESH	0x00	<39>	<38>	<37>	<36>	<35>	<34>	<33	<32>	write
0x49	RTCLG1_THRESH	0x00	<31>	<30>	<29>	<28>	<27>	<26>	<25>	<24>	write
0x4A	RTCLG1_THRESH	0x00	<23>	<22>	<21>	<20>	<19>	<18>	<17>	<16>	write
0x4B	RTCLG1_THRESH	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	write
0x4C	RTCLG1_THRESH	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x4D	CYCLPRESC	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x4E	CYCLTOP	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	write
0x4F	CYCLTOP	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x50	CNTR40	0x00	<39>	<38>	<37>	<36>	<35>	<34>	<33	<32>	read
0x51	CNTR40	0x00	<31>	<30>	<29>	<28>	<27>	<26>	<25>	<24>	read
0x52	CNTR40	0x00	<23>	<22>	<21>	<20>	<19>	<18>	<17>	<16>	read
0x53	CNTR40	0x00	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	read
0x54	CNTR40	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x55	CNTR40_CLR	0x00	--	--	--	--	--	--	--	<0>	write
0x56	FIFO_LENGTH	0x14	--	--	<5>	<4>	<3>	<2>	<1>	<0>	write
0x57	FIFO_COUNT_433	0x00	--	--	<5>	<4>	<3>	<2>	<1>	<0>	r/w
0x58	FIFO_COUNT_868	0x00	--	--	<5>	<4>	<3>	<2>	<1>	<0>	r/w
0x59	FIFO_COUNT_2G4	0x00	--	--	<5>	<4>	<3>	<2>	<1>	<0>	r/w
0x5A	RX_FIFO_5_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x5B	RX_FIFO_4_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x5C	RX_FIFO_3_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x5D	RX_FIFO_2_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x5E	RX_FIFO_1_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x5F	RX_FIFO_0_433	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x60	RX_FIFO_5_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x61	RX_FIFO_4_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x62	RX_FIFO_3_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x63	RX_FIFO_2_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x64	RX_FIFO_1_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x65	RX_FIFO_0_868	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x66	RX_FIFO_5_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x67	RX_FIFO_4_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x68	RX_FIFO_3_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x69	RX_FIFO_2_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x6A	RX_FIFO_1_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x6B	RX_FIFO_0_2G4	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read
0x6C	ACTUAL_NFA_433	0x25	--	NFA433_FAST<2>	NFA433_FAST<1>	NFA433_FAST<0>	--	NFA433_SLOW<2>	NFA433_SLOW<1>	NFA433_SLOW<0>	read
0x6D	ACTUAL_NFA_868	0x15	--	NFA868_FAST<2>	NFA868_FAST<1>	NFA868_FAST<0>	--	NFA868_SLOW<2>	NFA868_SLOW<1>	NFA868_SLOW<0>	read
0x6E	ACTUAL_NFA_2G4	0x25	--	NFA2G4_FAST<2>	NFA2G4_FAST<1>	NFA2G4_FAST<0>	--	NFA2G4_SLOW<2>	NFA2G4_SLOW<1>	NFA2G4_SLOW<0>	read
0x6F	ACTUAL_BANDSELECT	0x07	--	--	--	--	--	2G4	868	433	read
0x71	GENPURP_1	0x00	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	write
0x73	XTAL_OSC_CTRL	0x01	--	--	--	--	--	--	--	<0>	write
0x74	LDO_XTAL_CTRL	0x03	--	--	LDO_ENA_N	--	XTAL_OSC_BYP	--	INT<1>	INT<0>	write
0x75	MUX_D_OUT_SEL	0x0F	--	--	--	--	<3>	<2>	<1>	<0>	write
0x76	LC_TG_ENA	0x01	--	--	--	--	--	--	--	<0>	write
0x77	XTAL_GOOD	0x00	--	--	--	--	--	--	--	<0>	read
0x7C	KORREL_SV_CLEAR	0x00	--	--	--	--	--	--	--	<0>	write
0x7F	VERSION	0x41	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	read

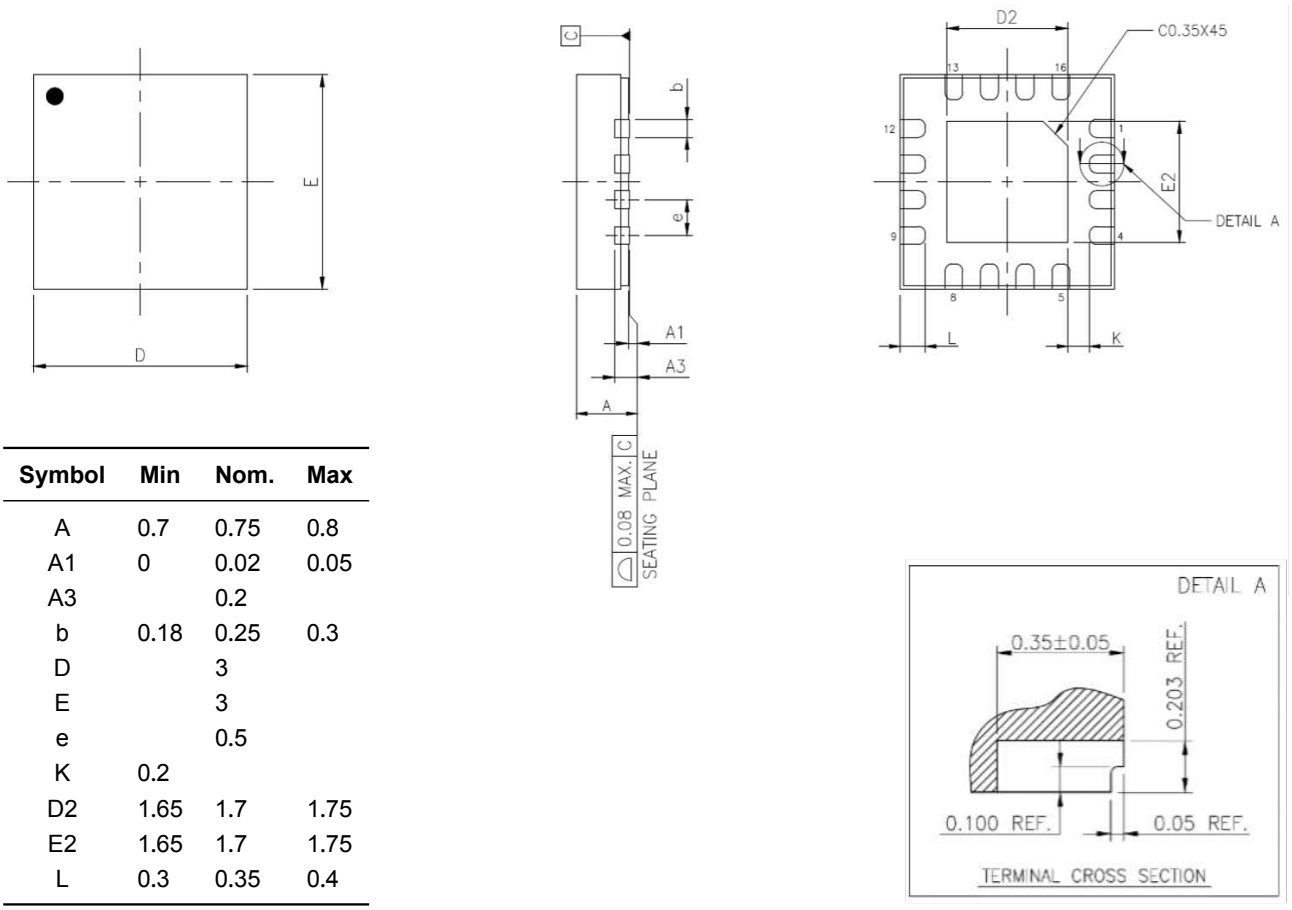
Table 31: Register Set.

8 Mechanical, Packaging and Order Information

The following pages include mechanical, packaging, and order information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

8.1 Chip Package Outline

QFN-16 3x3 with wettable flanks.



Symbol	Min	Nom.	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3		0.2	
b	0.18	0.25	0.3
D		3	
E		3	
e		0.5	
K	0.2		
D2	1.65	1.7	1.75
E2	1.65	1.7	1.75
L	0.3	0.35	0.4

Figure 19: Package outline drawing (dimensions in mm).

Lead-frame Material: C194 Copper-Iron Alloy

Lead-frame Finish: Pure Tin

8.2 Recommended Land Pattern (QFN-16 3x3)

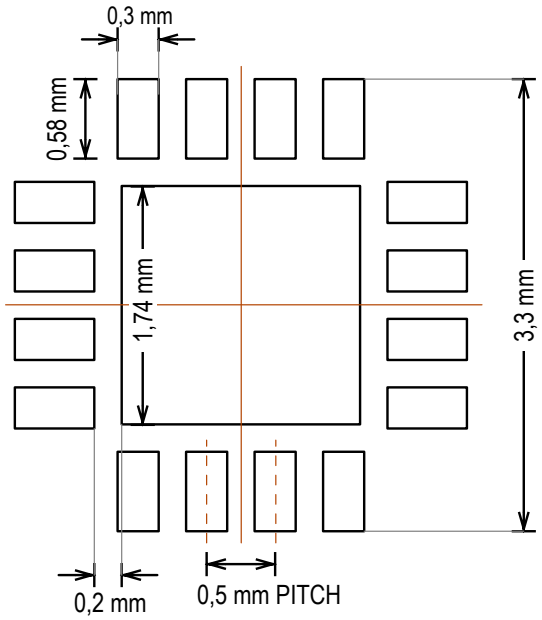


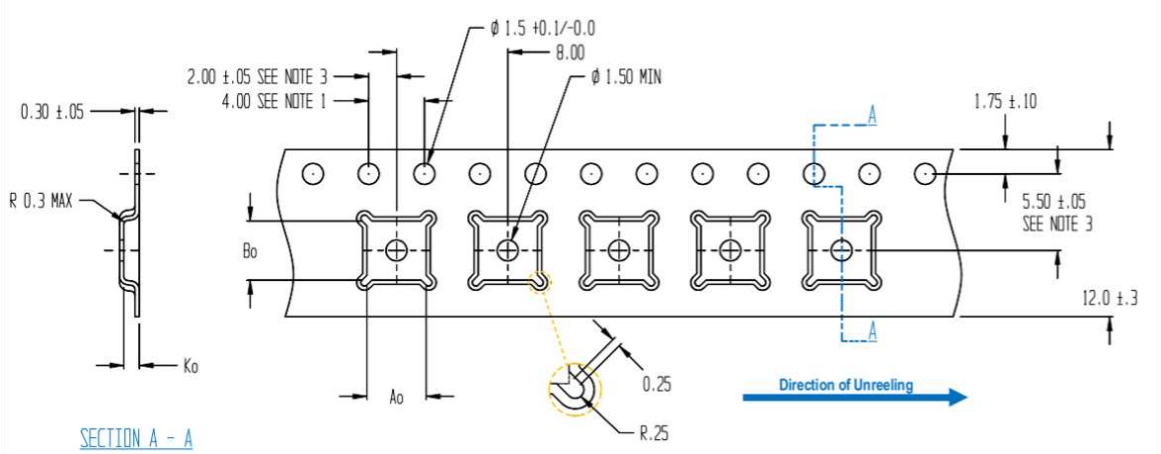
Figure 20: Recommended land pattern.

8.3 Chip Marking

Figure 21: Chip marking.

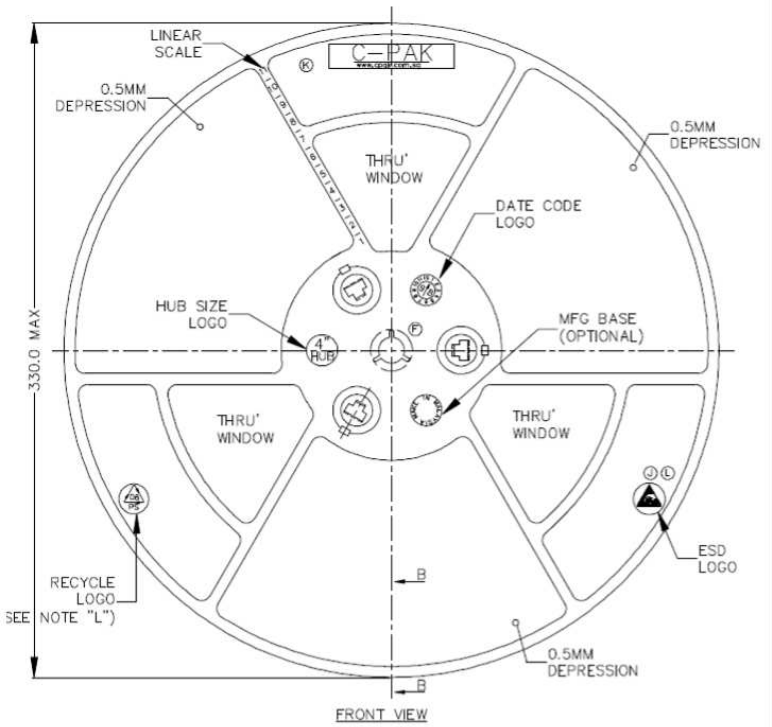
YY = Year
WW = Work Week
○ = Pin1 Designator

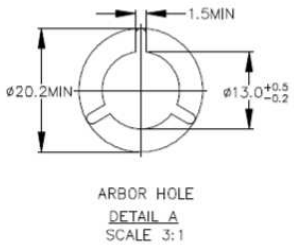
8.4 Tape & Reel Information



Note 1: Sprocket hole pitch cumulative tolerance ±0.2.
Note 2: Camber in compliance with EIAP481.
Note 3: pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
Note 4: All dimensions in mm.

Figure 22: T&R carrier tape.





Note 1: All dimensions in mm
Note 2: 16 mm reel's flanges are identical (Side A)
Note 3: Hub standard width (W): 12 mm

	SURFACE RESISTIVITY			
	LEGEND	SR RANGE	TYPE	COLOUR
	A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
G	B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
H	C	10^{5} AND BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
F	C	10^{5} TO 10^{9}	CONDUCTIVE (CUSTOM)	BLACK ONLY

Figure 23: 7" Reel drawing.

8.5 Order Information

Product	PACKAGE	BODY SIZE (NOM)	Pins	Qty. per Package	MSL[1]	Eco Plan[2]	Order No.
FH101RF	QFN-16	3.00 mm × 3.00 mm	16		1	Green (RoHS & no Sb/Br)	FH101RF

[1] MSL: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.
[2] Eco Plan: Green (RoHS & no Sb/Br): RM defines ”Green” to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1 % by weight in homogeneous material)

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9 Electrostatic Discharge Caution

Like most semiconductor devices RFicient® chips have limited built-in ESD protection. The product is distributed on reel in conductive tape & reel packaging which shorts all leads together. For SMT assembly great care must be applied to prevent any electrostatic charge on the devices leads. ESD damage can range from subtle performance degradation to complete device failure. In case of doubt, please refer to EBV for detailed instructions regarding proper ESD handling.

10 Trademarks and Licenses

RFicient® is a trademark of Fraunhofer Gesellschaft. This product is designed by and sold under license of Fraunhofer Gesellschaft.

Fraunhofer IIS

11 Sales Channel

This device is distributed worldwide by LZE GmbH

Sales Office: Frauenweiherstraße 15, 91058 Erlangen
Phone: **+49 (0) 9131 92894 80**
E-mail: contact@lze-innovation.de
Web: www.lze-innovation.de

12 Disclaimer

RFicient® devices are generally not allowed to be used

(a) In nuclear systems or nuclear facilities,
(b) In air traffic control, military applications,
(c) In weapons, application or system
(d) In critical applications where failure of the product could result in a situation where death, personal injury, or catastrophic property damage could occur
(e) In medical devices or medical tools
    a. intended to be surgically implanted in the human body
    b. intended to support or sustain human life
    c. in which a malfunction or failure of such application may result in injury or death to the patient.

Any liability, for any loss, damage and cost or expense arising out of or resulting from use of the product in cases (a) through (e) described above, is excluded.

13 Document Revision History

Date	Version	Comments/Changes
6.4.2023	1.3b	Initial release.